Core Generator Software System

After completing this module, you will able to:

- Describe the differences between LogiCORE™ and AllianceCORE solutions
- Identify two benefits of using cores in your designs
- Create customized cores by using the CORE Generator software system GUI
- Instantiate cores into your HDL design
- Run behavioral simulation on a design that contains cores

What are Cores?

- **A core is a ready-made function that you can instantiate into your design as a *black box***
- **Cores can range in complexity**
  - Simple arithmetic operators, such as adders, accumulators, and multipliers
  - System-level building blocks, such as filters, transforms, and memories
  - Specialized functions, such as bus interfaces, controllers, and microprocessors
- **Some cores can be customized**

Benefits of Using Cores

- **Save design time**
  - Cores are created by expert designers who have in-depth knowledge of Xilinx FPGA architecture
  - Guaranteed functionality saves time during simulation
- **Increase design performance**
  - Cores that contain mapping and placement information have predictable performance that is constant over device size and utilization
  - The data sheet for each core provides performance expectations
    - Use timing constraints to achieve maximum performance

Types of Cores

- LogiCORE solutions

- AllianceCORE solutions

LogiCORE Solutions

- **Typically customizable**
- **Fully tested, documented, and supported by Xilinx**
- **Many are pre-placed for predictable timing**
- **Many are unlicensed and provided for free with Xilinx software**
  - More complex LogiCORE solution products are licensed
- **VHDL and Verilog flow support for several EDA tools**

AllianceCORE Solutions

- **Point-solution cores**
  - Typically not customizable (some HDL versions are customizable)
- **Sold and supported by Xilinx AllianceCORE solution partners**
  - Partners can be contacted directly to provide customized cores
  - A free evaluation version of the module is available
    - You will need to contact the IP Center for licensing and ordering information
- **All cores are optimized for Xilinx; some are pre-placed**
- **Typically supplied as an Electronic Design Interchange Format (EDIF) netlist**
- **VHDL and Verilog flow support**

Sample Functions

- **LogiCORE solutions**
  - DSP functions
    - Time skew buffers, Finite Impulse Response (FIR) filters, transforms, and correlators
  - Math functions
    - Accumulators, adders, multipliers, integrators, trig functions, and square root
  - Memories
    - Pipelined delay elements, single- and dual-port RAM
    - Synchronous FIFOs
  - PCI™ core master and slave interfaces, PCI core bridge

- **AllianceCORE solutions**
  - Peripherals
    - DMA controllers, programmable interrupt controllers, and UARTs
  - Communications and networking
    - ATM, Fibre Channel, and Ethernet MAC
    - Error Correction
    - CTC, 3GPP, Viterbi, and Reed-Solomon
  - Video and image processing
  - Standard bus interfaces
    - PCMCIA, USB, PCI, PCI Express® core

CORE Generator Software System

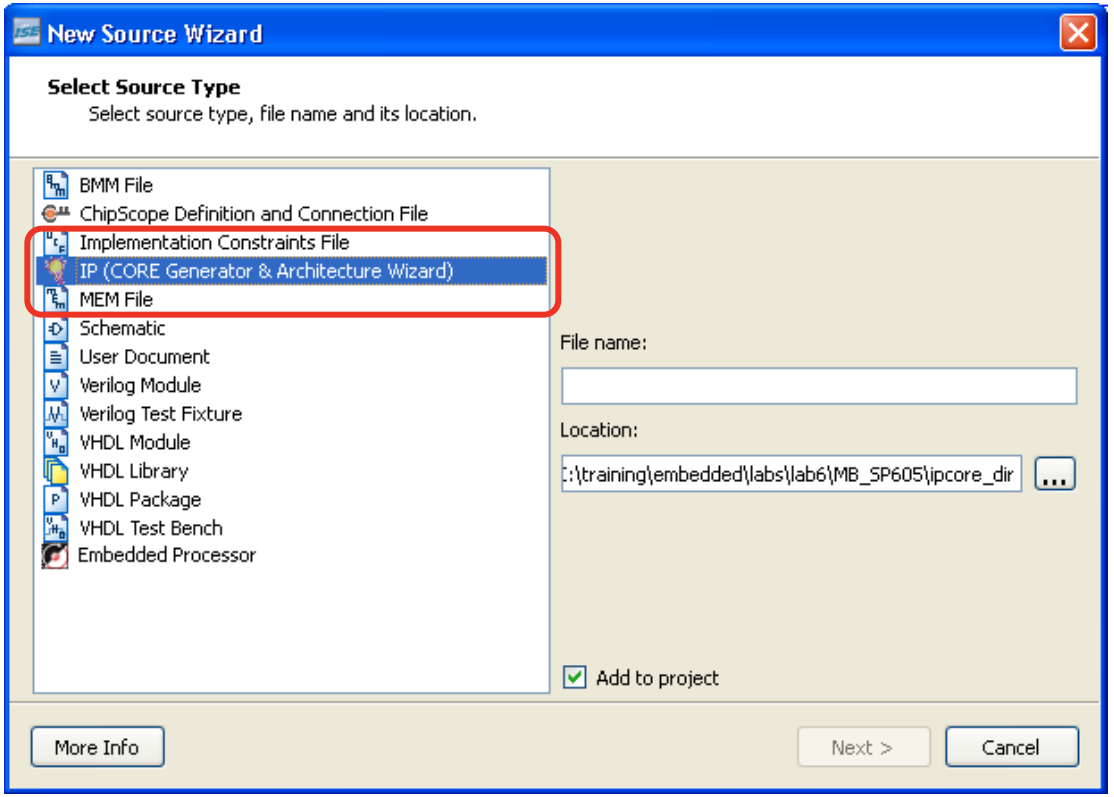
- **A Graphical User Interface (GUI) allows central access to LogiCORE IP products, as well as**
  - Data sheets
  - Customizable parameters
- **Interfaces with design entry tools**
  - Creates instantiation templates for HDL-based designs
- **Web Links tab provides access to the Xilinx Website and the IP Center**
  - The IP Center contains new cores to download and install
    - You always have access to the latest cores

Launching the CORE Generator

- The Core Generator is available as standalone application
  - Launched from Programs → Xilinx ISE Design Suite→ ISE Design Tools→ Tools → Core Generator
- Can be launched from ISE Project Navigator.
- Latest 12.1 PlanAhead software has Core Generator software integrated.

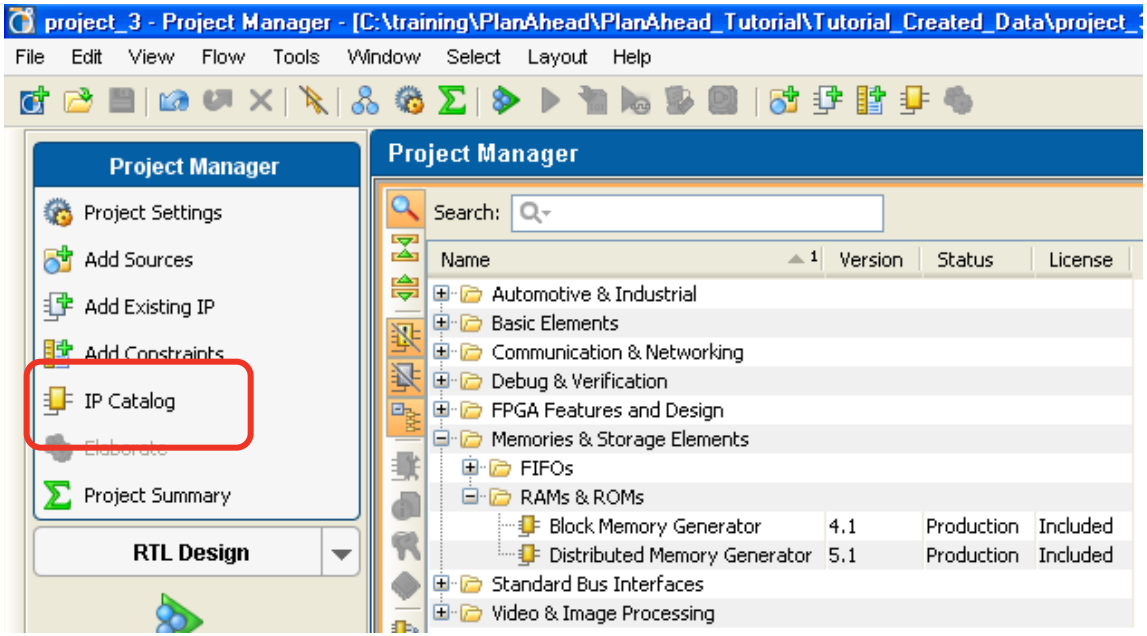
Running the CORE Generator

- From the Project Navigator, select *Project → New Source*
- Select *IP (CORE Generator & Architecture Wizard)* and enter a filename
- Click *Next* and then select the type of core

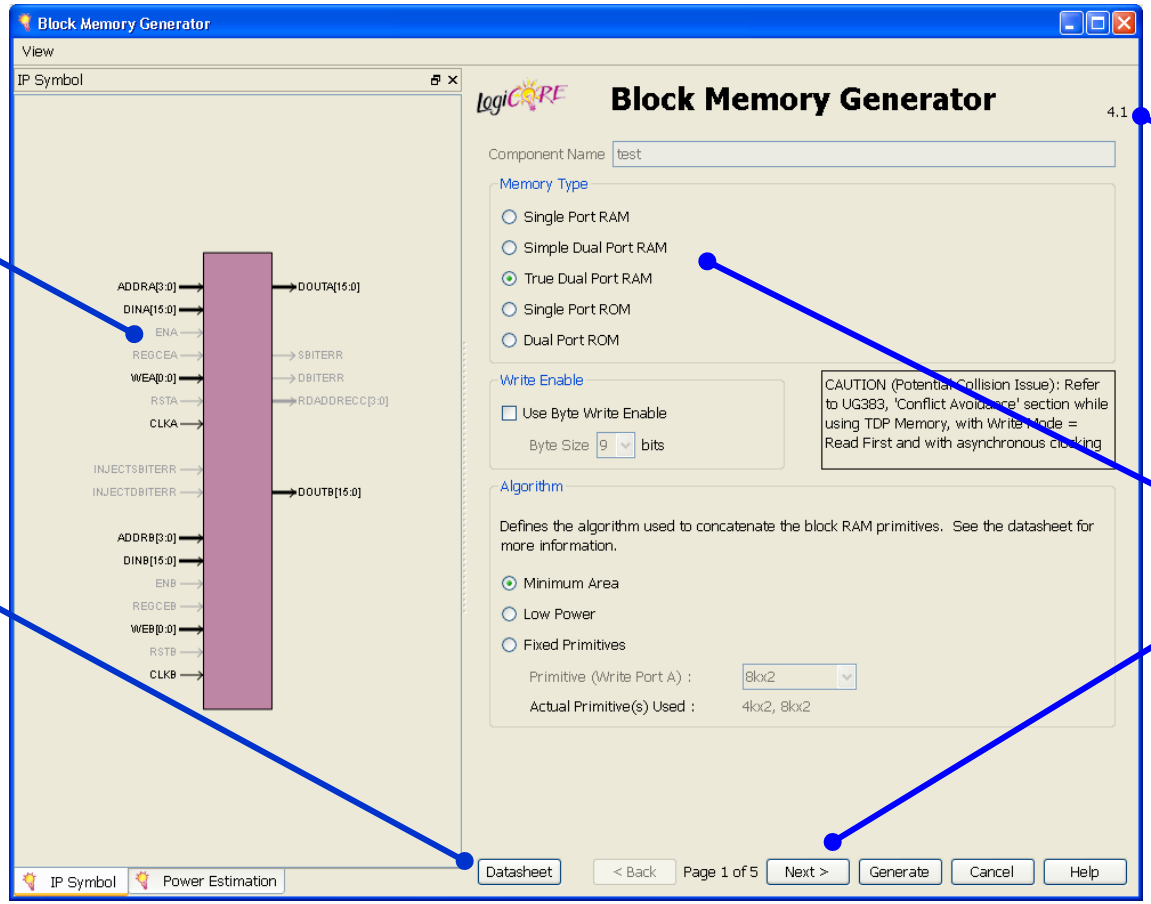


Running the CORE Generator(contd)

- From the PlanAhead GUI , select *Project Manager→ IP Catalog.*
- In IP Cores window expand tree and select the type of core.



Core Customize Window



Symbol (unused ports grayed out)

Data sheet access

Version information

Customizable parameters spread over several dialog boxes

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Core Data Sheets

Features

Also: Functionality and pinout (next page)

Performance expectations and resource utilization

XILINX® LogiCORE™

Block Memory Generator v3.3

DS512 September 16, 2009 — **Product Specification**

Introduction

The Xilinx LogiCORE™ IP Block Memory Generator core is an advanced memory constructor that generates area and performance-optimized memories using embedded block RAM resources in Xilinx FPGAs. Available through the CORE Generator™ software, users can quickly create optimized memories to leverage the performance and features of block RAMs in Xilinx FPGAs.

Features

- Generates Single-port RAM, Simple Dual-port RAM, True Dual-port RAM, Single-port ROM, and Dual-port ROM
- Performance up to 450 MHz
- Supports data widths from 1 to 1152 bits and memory depths from 2 to 9M words (limited only by memory resources on selected part)
- Supports configurable port aspect ratios for dual-port configurations and read-to-write aspect ratios in Virtex®-6, Virtex-5 and Virtex-4 FPGAs
- Optimized algorithms for minimum block RAM resource utilization or low power utilization
- Configurable memory initialization
- Supports individual write enable per byte in Virtex-6, Virtex-5, Virtex-4, Spartan®-6, and Spartan-3A/XA DSP with or without parity
- Optimized VHDL and Verilog behavioral models for fast simulation times; structural simulation models for precise simulation of memory behaviors
- Selectable operating mode per port: WRITE_FIRST, READ_FIRST, or NO_CHANGE
- Supports built-in Hamming Error Correction Capability (ECC) for Virtex-6 and Virtex-5 devices, and associated error injection pins in Virtex-6 to insert single and double bit errors
- Supports pipelining of DOUT bus for improved performance in specific configurations
- Smaller primitive configurations in Spart devices with the introduction of new 9K primitives.
- Lower data widths for Virtex-6 devices in SDP mode.
- Choice of reset priority for output registers between priority of SR (Set Reset) or CE (Clock Enable) in Spartan-6 and Virtex-6 families.
- Asynchronous reset in Spartan-6 devices.

LogiCORE™ IP Facts	
Core Specifics	
Supported Device Family (1)	Virtex-6, Virtex-5, Virtex-4, Spartan-6, Spartan-3E/XA, Spartan-3/XA, Spartan-3A/3AN/3A DSP
Block RAM	Varied, based on core parameters
DCM	None
BUFG	None
IOBs/ Transceivers	None
PPC	None
IOB-FF/TBUFs	None
Provided with Core	
Documentation	Product Specification Migration Guide (2)
Design File Formats	NGC Netlist
Design Tool Requirements	
Xilinx Implementation Tools	ISE® v11.3
Simulation	Mentor Graphics® ModelSim®: v6.4b and above VHDL Structural Verilog Structural VHDL Behavioral (3) Verilog Behavioral (3)
Synthesis	XST
Support	
Provided by Xilinx, Inc.	

1. See Table 1, page 2 for more details about supported devices.
2. The Migration Guide provides instructions for converting designs that contain instances of either Legacy LogiCORE IP 6.x Single or Dual Port Block Memory, or older versions

Memory Type	Options	Width x Depth	Resource Utilization						Performance (MHz)
			Block RAMs			Shift Regs	FFs	LUTs (1)	
			36K	16K	8K				
True Dual-port RAM	No Output Registers	36x512	1	0	0	0	0	0	325
		9x2k	0	1	0	0	0	0	325
	Embedded Output Registers	36x512	1	0	0	0	0	0	450
		9x2k	0	1	0	0	0	0	450

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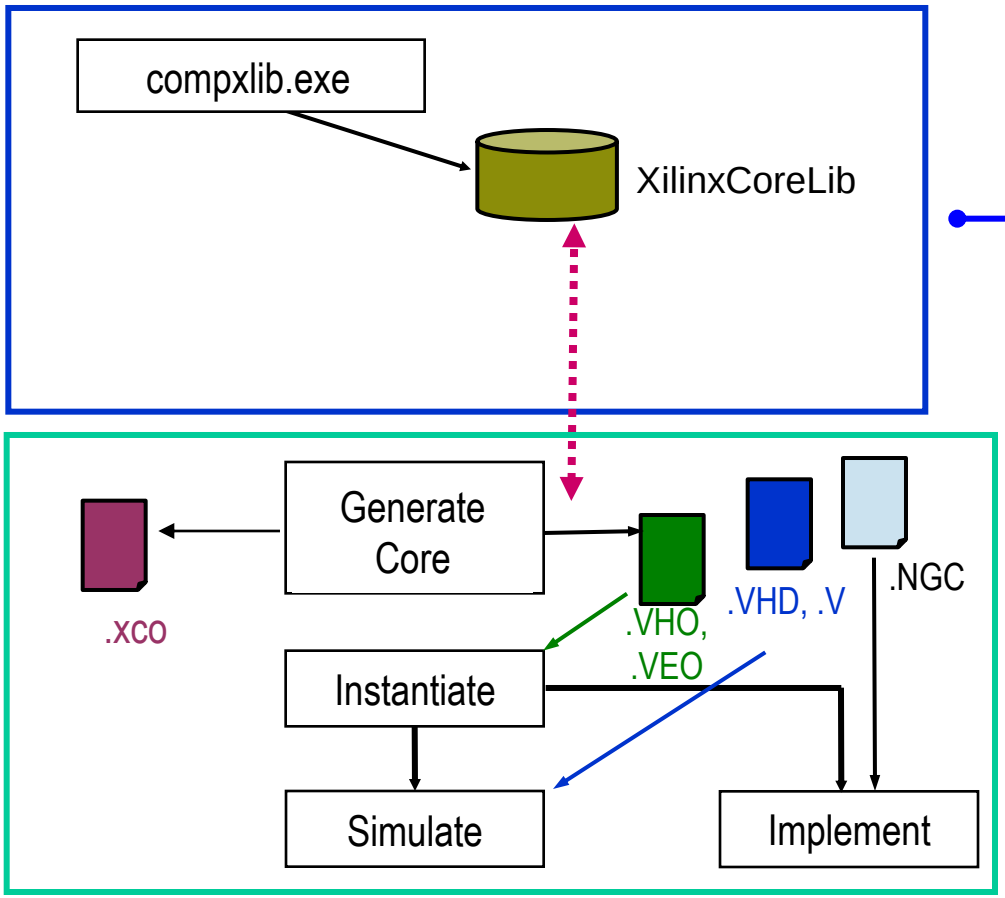
HDL Design Flow



Compile library for behavioral simulation (one time only)

Core generation and integration

Core Generation and Integration

- **Generate or purchase a core**
  - Netlist file (NGC)
  - Instantiation template files (VHO or VEO)
  - Behavioral simulation wrapper files (VHD or V)
- **Instantiate the core into your HDL source**
  - Cut and paste from the templates provided in the VEO or VHO file
- **The design is ready for synthesis and implementation**
- **Use the wrapper files for behavioral simulation**
  - The ISE® software automatically uses wrapper files when cores are present in the design
  - VHDL: Analyze the wrapper file for each core before analyzing the file that instantiates the core

Summary

- A core is a ready-made and verified function that you can insert into your design
- LogiCORE solution products are sold and supported by Xilinx
- AllianceCORE solution products are sold and supported by AllianceCORE solution partners
- Using cores can save design time and provide increased performance
- Cores can be used in schematic or HDL design flows

Where Can I Learn More?

- **Xilinx IP Center**
  - **Help → Xilinx on the Web → IP Center**
    - Find out about new IP (for EDK as well)
    - Browse IP by type, vendor, and function
    - Find IP documentation
    - Update the Core Generator with the latest IP
    - Evaluate IP
- **Xilinx Training**
  - www.xilinx.com/training
    - Xilinx tools and architecture courses
    - Hardware description language courses
    - Basic FPGA architecture, Basic HDL Coding Techniques, and other free training videos!