Tutorial 2 Automatic Placement & Routing

Please follow the instructions found under <u>Setup</u> on the <u>CADTA main page</u> before starting this tutorial.

1.1. Start Encounter

Log on to a VLSI server using your EE departmental username and password. Go to your Encounter directory by typing:

cd ~/cad/se

cp your mapping verilog file without header and output lef file from previous tutorial and via fix pearl code:

cp ~/cad/cadence/ABSOutput.lef.

cp /home/cad/startup/EE6325/aux/addvias.pl .

Source the proper profile:

. /proj/cad/startup/profile.ic-5

Start the Encounter design environment by typing the following in your Encounter directory:

If you are on apache:

/proj/cad/cadence/edi_test/edi-11.10.000.sun4v/bin/encounter

If you are on txace:

/proj/cad/cadence/edi_test/edi-11.10.000.lnx86/bin/encounter

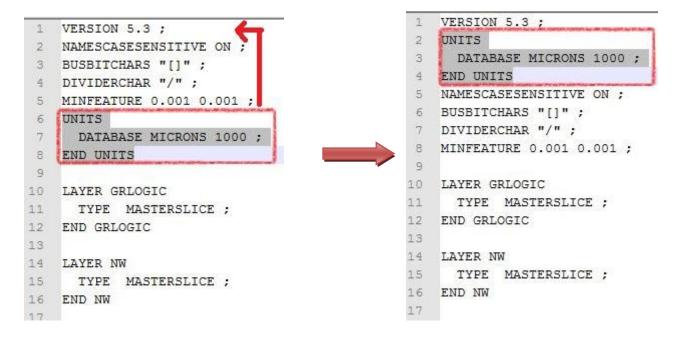
(MAKE SURE YOU DO NOT RUN THIS IN BACKGROUND !!!)

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1.2. Import files

Before you import the LEF file, you will need to modified your LEF file a little bit, so that the Encounter11.1 can read your LEF file correctly.

Open the ABSOuput.lef, find "DATABASE MICRONS 1000 " part, cut this whole part and paste it in the beginning of LEF file just like following. Save the file.



Now you can import both your Cadence LEF file (which contains information that Encounter needs regarding your cell library) and your synthesized Verilog netlist (which contains an electrical description of the circuit) into the Silicon Ensemble environment.

In the Encounter GUI, Click *File -> Import Design*, the Design Import window will pop up.

In the Netlist part, check *Verilog* option, select your verilog file for, and check *Auto Assign* option for Top Cell.

In the Technology/Physical Libraries part, check *LEF Files* option, select your ABSOuput.lef file.

In the Power part, put vdd! and gnd! for Power/Ground Nets . and then Click OK

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Verilog		
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Floorplan		
IO Assignment File		0
Power		
Power Nets	vddl	
Ground Nets	gndl	
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	Create Analysis Configuration	

1.3. Floorplanning

Floorplanning is the stage of the design where the area of the design is defined. Two regions exist within the design: the core, which contains the cells arranged in rows, and the I/O area, which contains power and ground rings and I/O pins.

Select Floorplan -> Specify Floorplan to open the *floorplanning* window. In the *Basic* tab. Make sure *Core Size* is set to *Aspect Ratio* and *Aspect Ratio* is set to **1.0** (this controls the ratio between height and width of the design). Set the *Core to IO Boundary Distance* to 20 microns all directions. (If the design has room after routing, you may want to go back and re-run floorplanning with a smaller distance, as this will reduce the area of your design substantially. This will mean however that you will need to re-run all steps after floorplanning as well).

Do **NOT** click OK now.

pecify By: 🧕 Size 🔾 Die/IO/Core C	oordinates	
● Core Size by: ● Aspect Ratio:	Ratio (H/W):	1
e	Core Utilization:	0.700001
	Cell Utilization:	0.700001
Dimension:	Width:	273.58
	Height:	263.2
◯ Die Size by:	Width:	273.58
	Height:	263.2
Core Margins by: • Core to IO Bou	ndary	
Core to Die Bo	undary	
Core to Left: 20	Core to Top:	20
Core to Right: 20		20
Die Size Calculation Use: O Max I		
Floorplan Origin at: 💿 Lower	Left Corner 🔾 Cen	ter Unit: Micror
		onn. mileroi

Then, go to the *Advanced* tab. Change your *Double-back rows* as picture. The *Row Spacing* setting controls the distance between rows of cells (space where routing can occur on the metal1 layer) and should be initially set to several microns. It may be possible to later reduce this distance to shrink the design area, but it is necessary to view the routed design to determine this first. Make sure the *Bottom IO Pad Orientation* as picture. Click **OK** to finalize the floorplan.

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	ping Same Site Ro			
- IO Specifications	.			
Bottom IO Pad Ori	entation: 🔲 R0			
Use I/O Rows fo	or I/O Placement			
	ox to Grid			

And after floorplanning, your Encounter will looks like this. (You can use key "F" to zoom fit)

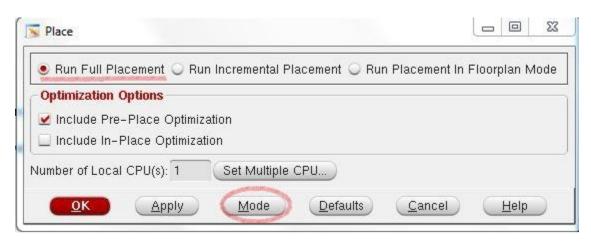
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1.4. Placement

1.4.1. Place Standard Cells

Once the floorplanning is complete, IO ports and cells need to be placed in the alotted rows.

Select *Place -> Place Stand<u>a</u>rd Cells*. In the Place window, make sure *Run Full Placement* is selected. Do **NOT** click OK now. Click <u>Mode</u>.



And the Mode Setup window will show like following. Select *Placement* in the List of Modes, use *Medium* for Congestion Effort. Since we do not do the timing analysis and power analysis, we do not need all these options. Just make sure *Place IO Pins* is selected. Click *OK*.

Mode Setup		
CTS	Placement Mode Placement RefinePlace	
ClockMesh Filler NanoRoute Optimization Flacement ScanReorder StreamOut OasisOut TieHiLo TrialRoute	Congestion Effort Low Medium High Auto Run Placement In FloorPlan Mode Run Timing Driven Placement Enable Module Plan Enable Clock Gating Awareness Enable Power Driven Ignore Scan Connections Reorder Scan Connection Ignore Spare Cell Connections Place IO Pins Hierarchy Aware Spare Cell Placement Specify Maximum Density Layers Checked For Pin Access 1 Select Specify Maximum Routing Layer 1 Set Defaults	
	<u>OK</u> <u>Apply</u> <u>Cancel</u> <u>H</u> elp	

Now, you can click **OK** in your Place window. The Encounter will show like following. (This process may take a while)

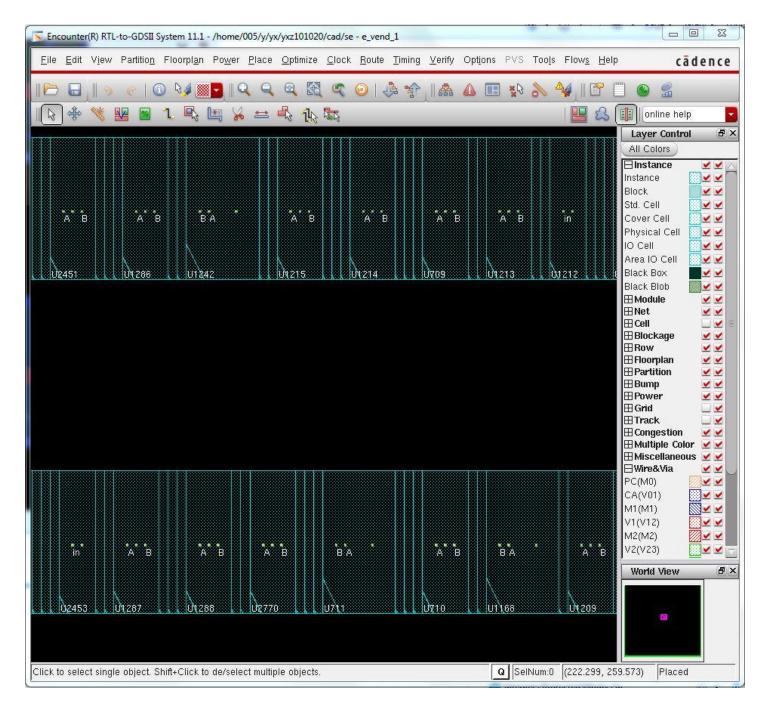
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1.4.2. Place Fillers between cells

If you have filler in your library, place the filler right now. Select <u>Place -> Physical Cells -> Add Filler</u>. The Add Filler window will pop up. Select your filler's name in the Cell Name(s). If you used different name for filler, put the right name there. Click OK.

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Cell Name(s) filler	(Select)
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Power Domain	Select
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<u>OK</u> <u>Apply</u> <u>M</u> ode <u>C</u> ancel	I) <u>H</u> elp

Then try to change your zoom or move the view, you will see the fillers.



As you see there is no space between cells.

1.5. Power/Ground

1.5.1. Tie-hi and Tie-lo nets

Since there are no Tie-hi/Tie-lo cells in the library, you need to connect between the Tie-hi and Tie-lo nets to the appropriate power and ground net. These are keywords in the Verilog netlist, such as 1'b0, 1'b1.

Select *Power -> Connect Global Nets,* the *Global Net Connections* window will pop up.

Select *Tie High* in the Connect part, Select *Apply All* in Scope part, put *vdd!* In To Global Nets, click *Add to List*. Then you will see "vdd!:TIEHI:*.:ALL" in the left Connection List.

Select *Tie Low* in the Connect part, Select *Apply All* in Scope part, put *gnd!* In To Global Nets, click *Add to List*.

The window should looks like this:

vddl:TIEH:*.All gndl:TIELO:*::All Pin Tie High Tie Low Instance Basename: * Pin Name(s): Net Basename: Scope Single Instance: Under Module: Under Power Domain: Under Region: Ik: 0.0 Instance Region: Ik: 0.0 Apply All To Global Net: gnd! Override prior connection Verbose Output Add to List Update Delete	Connection List	Power Ground Connection	
Scope Single Instance: Under Module: Under Power Domain: Under Region: IIx: 0.0 IIIy: 0.0 urx: 0.0 ury: 0.0 is Apply All To Global Net: gnd! Override prior connection Verbose Output	vddl:TIEHI:*.:All gndl:TIELO:*.:All	 Pin Tie High Tie Low Instance Basename: * Pin Name(s):	
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Click **Apply**, then Click **Check**, there should be no error in your terminal. Close the window.

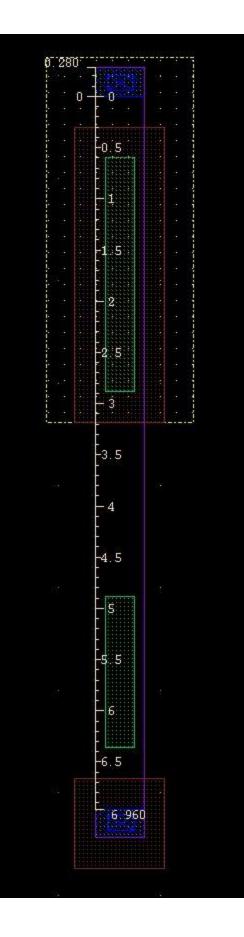
Select *Power -> Power Planning -> Add <u>Ring</u>*, the *Add Rings* window will pop up.

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2.0		2.4	2.4	2.4		
A	t ———					
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Make sure your power and ground net names (**vdd! gnd!**) appear in the *Nets* window (you can select the net names with the button beside), set the *Width* to **0.4** microns, the *Spacing* to **0.4** microns, and make sure the *Offset* parameters are set to **Specify**. For offset, PUT some number with on grid. If your grid is 0.48, put 2.4 or 4.8 or some number (n* grid). Click **OK** to apply the rings and close the *Plan Power* window.

Selcet *Power -> Power Planning -> Add Stripe*, the *Add Stripe* window will show.

Make sure (vdd! gnd!) appear in the *Nets* window again. Change Layer to M1. Change Direction to Horizontal. Width is supposed to be equal to your vdd and gnd M1 width in your cells. Spacing is equal to the space between vdd! and gnd! Trail.



Set Pattern needs to be checked at Number of sets and put the number of rows you have in your design, then Click **OK**.

Set Conf	iguration
Net(s):	gndl vddl
Layer:	M1 >
Direction:	🔾 Vertical 💿 Horizontal
Width:	0.28
Spacing:	6.96
Set Patt	em
🔾 Set-to-	-set distance: 100
🖲 Numbe	r of sets: 23
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🔾 Over P	/G pins Pin layer: Top pin layer 🕨 🗌 Max pin width: 0
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Now you encounter should looks like this:

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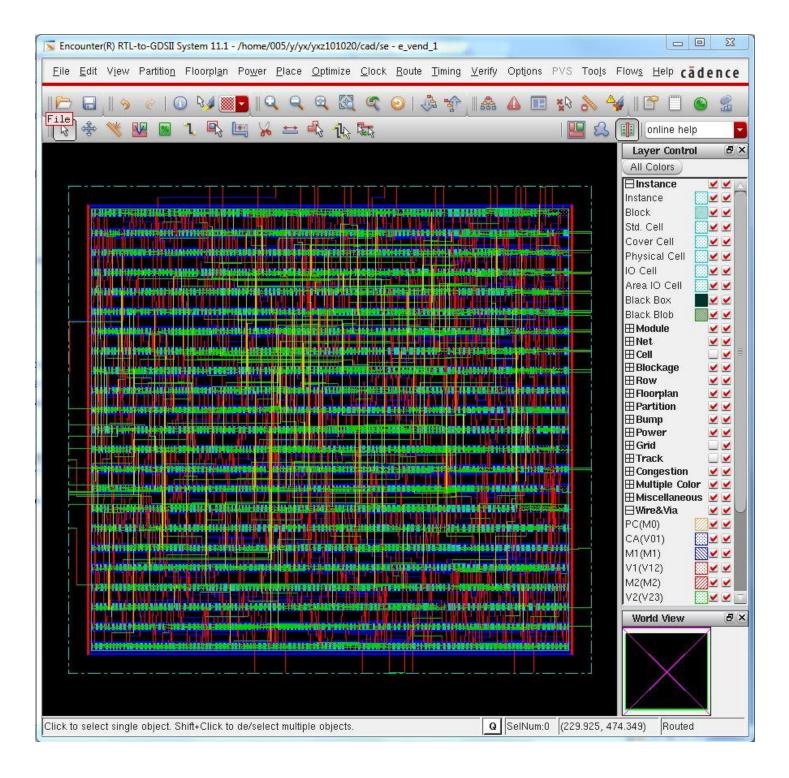
1.6. Routing

Now we will connect the cells together and to the I/O pins by routing the circuit nets. Select <u>Route -></u> <u>NanoRoute -> Route</u>, make sure **Global Route** and **Detail Route** is selected, and click **OK**.

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Post Route Optimization	n 🔲 Optimize Via 🔲 Optimize Wire
Concurrent Routing F	eatures
🗹 Fix Antenna	🔲 Insert Diodes 💿 Diode Cell Name
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SI Driven	
Post Route SI	SI Victim File
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📃 Post Route Litho Re	pair
Routing Control	
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🗹 Auto Stop	
Number	r of Local CPU(s): 1
Number of CUP(s) per	Remote Machine: 1
and the second se	mote Machine(s): 0
Set Multiple CPU	

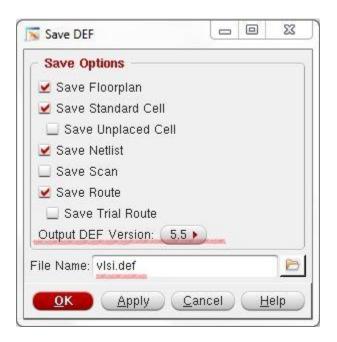
This process may take a while. When it is complete you should have wires connecting your pins together:

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1.7. Export files

Finally, we need to export a DEF format file for Cadence. This file contains physical cell placement and automatic routing information as well as electrical net information. Select <u>File -> Save -> DEF</u> from the main menu, change the **Output DEF Version** to **5.5**, fill in an appropriate file name, and then click **OK**.



1.8. Exit Encounter

Select <u>File -> Exit</u>.

1.9. Run ADDVIAS code

Your DEF file missing some Vias for your layout, so you have to run this script to add vias in your def file

addvias.pl YOUR_DEF_FILE.def YOUR_DEF_FILE_VIAS.def

If it appers "command not found", try source it again

. /proj/cad/startup/profile.ic-5

addvias.pl YOUR_DEF_FILE.def YOUR_DEF_FILE_VIAS.def