Curriculum Vitae

Reza M. Rad

Contact:
Phone: 410-455-8776
Email: reza2@umbc.edu
Mail: 1000 Hilltop Circle, UMBC, ITE374
Baltimore, MD 21250

Education

Ph.D. Computer Engineering, 2008
Thesis Title: Detection and Localization of Hardware Trojans through Analysis of Power Ports Transient Signals
University of Maryland Baltimore County, Baltimore, MD

M.S. Computer Engineering,
1998-2001, University of Tehran, Tehran, Iran

Bachelor of Engineering (B.E.), Electrical Engineering (Communications)
1994-1998, University of Tehran, Tehran, Iran

Employment

Hardware Design Engineer,
IGI Technologies Inc., 2008-present

Lecturer, September 2008- Present
Department of CSEE, University of Maryland Baltimore County (UMBC)

Research Assistant and part time Lecturer, May 2005 – September 2008
Department of CSEE, University of Maryland Baltimore County (UMBC)

Lecturer, September 2001 – May 2005
BuAli Sina University, Iran

Research Assistant, June 1999 - September 2001
VLSI Circuits and Systems Laboratory, ECE Department, University of Tehran

FPGA Design Engineer, June 1997 - June 1999

Iran Telecommunication Research Center (ITRC)

Awards

R. M. Rad and C. Patel, "Innovative Ideas Based on Reconfigurable Systems on Chip", Kauffman Faculty Innovation Grant, 2009-2010, $6000

Publications

Journals

R. M. Rad and J. Plusquellic, "Gate Level Localization of Hardware Trojans Based on Temporal and Statistical Analysis of Power Supply Transient Signals", submitted to Journal of Electronic testing Theory and Applications (JETTA), 2009

R. M. Rad, J. Plusquellic, M. Tehranipoor, "An Evaluation of Power Signal Methods for Detecting Hardware Trojans under Real Process and Environmental Conditions", accepted for publication in IEEE Transactions on VLSI Systems, 2009.

R. M. Rad and Jim Plusquellic, "A Novel Fault Localization Technique Based on Deconvolution and Calibration of Power Pad Transients Signals", Journal of Electronic Testing Theory and Applications, 2008, pp. 169-185, vol. 25, No 2-3, June 2009.

R. M. Rad and M. Tehranipoor, "Evaluating Area and Performance of a Hybrid FPGA with Nanoscale Clusters and CMOS Routing", ACM Journal on Emerging Technologies in Computing Systems (JETC), vol. 3, issue 3, no. 15, 2007.

R. M. Rad and M. Tehranipoor, "SCT: A Novel Approach For Testing and Configuring Nanoscale Devices," *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, vol. 4, issue 3, no. 14, 2008.

M. Tehranipoor and **R. M. Rad**, "Built-in Self-Test and Recovery Procedures for Molecular Electronics-Based NanoFabrics," *IEEE Transactions on Computer Aided Design of Integrated Circuits*, vol. 26, no. 5, pp 943-958, 2007.

M. Tehranipoor and **R. M. Rad**, "Defect Tolerance for Nanoscale Crossbar-based Devices", IEEE Design & Test of Computers, vol. 25, issue 6, 2008.

Book Chapter

M. Tehranipoor and **R. M. Rad**, "Test and Defect Tolerance for Reconfigurable Nanoscale Devices", in *"Emerging Nanotechnologies: Test, Defect Tolerance, and Reliability"* by Mohammad Tehranipoor, Springer, 2007.

Conferences

R. M. Rad, X. Wang, J. Plusquellic, M. Tehranipoor, "Power Supply Signal Calibration Techniques for Imroving Detection Resolution to Hardware Trojans", IEEE Interantional Conference of Computer Aided Design (ICCAD), 2008.

R. M. Rad, J. Plusquellic, M. Tehranipoor, "Sensitivity Analysis to Hardware Trojans using Power Supply Transient Signals", IEEE Int. Workshop on Hardware Oriented Security and Trust, pp. 3-7, 2008.

R. M. Rad and Jim Plusquellic, "Temporal Analysis and Spatial Deconvolution of Power Pad Transients Signals for Fault Localization", IEEE workshop on defect based testing (DBT'07), 2007.

R. M. Rad and M. Tehranipoor, "A Reconfiguration-based Defect Tolerance Method for Nanoscale Devices", IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT'06), pp. 107-115, 2006.

R. M. Rad and M. Tehranipoor, "A New Hybrid FPGA with Nanoscale Clusters and CMOS Routing", in proc. of ACM IEEE Design Automation Conference (DAC), pp. 727-730, 2006.

R. M. Rad and M. Tehranipoor, "Investigating Test Time, Defect Map Size and Area for LUT and PLA-based Implementation of Nanoscale Devices", IEEE North Atlantic Test Workshop (NATW), 2006.

R. M. Rad and M. Tehranipoor, "SCT: An Approach for Testing and Configuring Nanoscale Devices", in proc. of IEEE VLSI Test Symposium (VTS06), pp. 370-377, 2006.

M. Tehranipoor and **R. M. Rad**, "Fine-Grained Island Style Architecture for Molecular Electronic Devices", in proc. of ACM/ SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA'06), Poster, page 226, 2006.

M. Tehranipoor and **R. M. Rad**, "Test and Recovery for Fine-Grained Nanoscale Architectures", in proc. of ACM/ SIGDA International Symposium on Field-Programmable Gate Arrays (FPGAí06), Poster, page 226, 2006.

G. R. Chaji, **R. M. Rad**, S. M. Fakhraie and M. H. Tehranipour, eUTDSP: A Design Study of a New VLIW-Based DSP Architecture, in proc. IEEE International Symposium on Circuits And Systems (ISCASí03), Bangkok, Thailand, vol. 4, pp. 137-140, 2003.