Single Electron Devices for Logic Applications

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Based on pages 425-441 of “Nanoelectronics and Information Technology”, Rainer Waser

Introduction

- Scaling down MOSFETs has been fundamental in improving the performance of ULSI circuits
- Scaling of MOSFETs is entering the deep sub 50 nm regime
- Quantum mechanical effects are expected to be effective in these small structure devices

Introduction

- A new device having operation principles effective in smaller dimensions which utilizes quantum-mechanical effects
- Single electron devices retain their scalability even on an atomic scale
- Single electron devices will reduce the power consumption because the number of electrons transferred from voltage source to ground is limited

Single-electron box

- A quantum dot connected with two electrodes
- One electrode connected to dot through a tunneling junction
- The other electrode, gate, coupled with quantum dot via insulator, electron cannot pass through tunneling

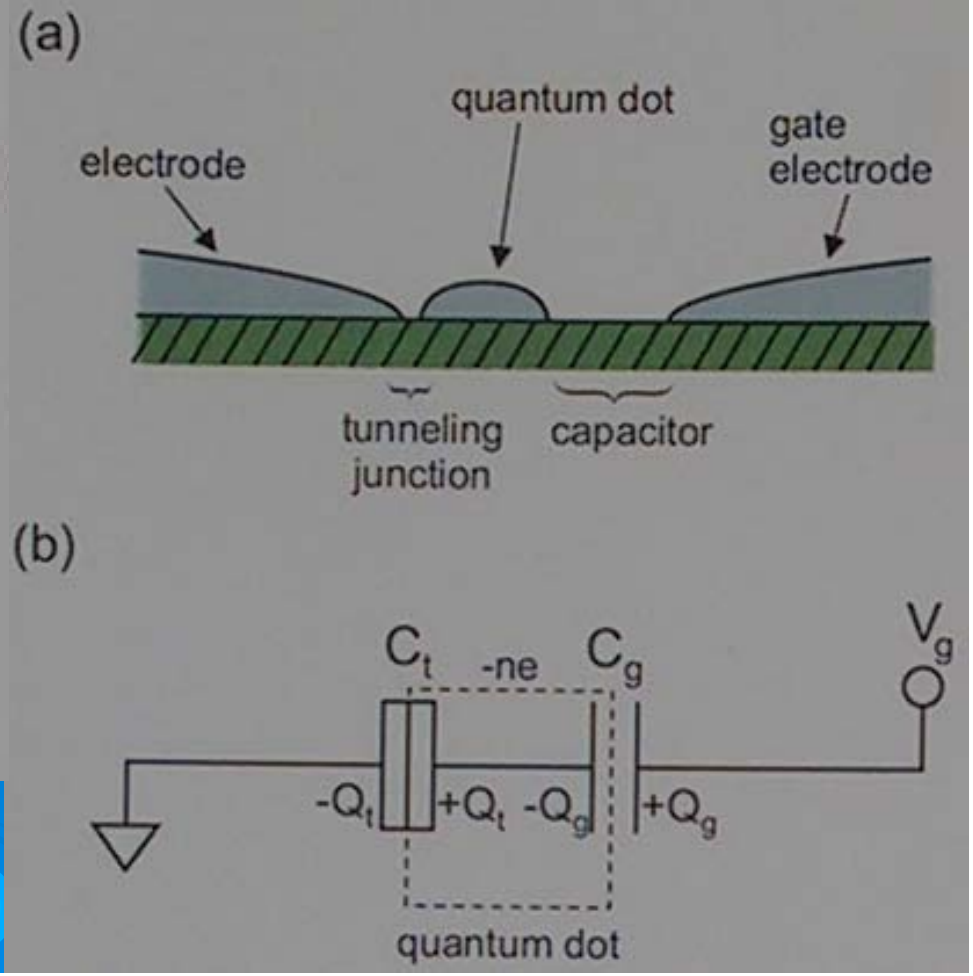
Single-electron box

- Electrons are injected/ejected to/from the dot through the tunneling junction (fig 1)

Figure 1:

(a) Schematic structure of single-electron box. The single-electron box consists of a quantum dot, an electrode connected to the dot through a tunneling junction, and an electrode coupled to the dot through an ideal, infinite-resistance, capacitor.

(b) Equivalent circuit of single-electron box.



Single-electron box

- **Basic operation of single-electron box:**

  - As the size of quantum dot decreases, charging energy Wc of a single excess charge on the dot increases
  - If Wc is sufficiently larger than thermal energy, no electron tunnels to/from quantum dot

  - Electron number in the dot takes a fixed value
  - The charging effect which controls injection/ejection of a single charge to/from a quantum dot is called **Coulomb Blockade** effect

Single Electron Devices

- Condition for Coulomb blockade:

$$W_c = \frac{e^2}{2C} >> k_B T$$

- By applying a positive bias to the gate electrode we could attract an electron to the quantum dot
- Further increase of the gate voltage causes an electron to enter the dot
- In single-electron box, the electron number of the box is controlled, one by one, by utilizing the gate electrode

Single-electron box

- Conditions for observing single-electron tunneling phenomena
  - First: charging energy of a single electron to the dot must be greater than thermal energy
  - Second: tunneling resistance R_t of the tunneling junction must be larger than resistance quantum h/e^2
  - This is required to suppress the quantum fluctuations in electron number, n, of the dot

Single-electron box

- This condition is obtained as follows:

Uncertainity principle:

$$\Delta W.\Delta t > h$$

let ΔW be the charging energy of the quantum dot:

$$\Delta W \approx e^2 / C$$

let Δt be the lifetime of the charging: $\mathrm{R_t C}$

Then: $(e^2 / C).\mathrm{R_t C} = e^2 R_t > h$

$$R_t >> \frac{h}{e^2} \approx 25.8\,\mathrm{k\Omega}$$

Single-electron box

- Bias conditions for Coulomb Blockade Effects
  - The voltage range which keeps electron number at n, is extracted by considering the free energy of the system
    - F(n) free energy having n electrons in the island
    - Wc(n) : Charging energy
    - A(n) : Work done by the voltage source connected to gate in order to change the electron number from 0 to n
    - Polarization charge in capacitors: due to rearrangement of electrons

$$F(n) = W_c(n) - A(n)$$

$$Q_t - Q_g = -ne$$

$$\frac{Q_t}{C_t} + \frac{Q_g}{C_g} = V_g$$

Q_t and Q_g are the polarization charge on the tunneling junction and gate capacitors

Single-electron box

- Bias conditions ..

$$W_c(n) = \frac{Q_t^2}{2C_t} + \frac{Q_g^2}{2C_g} = \frac{e^2 n^2}{2C_\Sigma} + \frac{1}{2}\frac{C_t C_g V_g^2}{C_\Sigma}, C_\Sigma = C_t + C_g$$

$$A(n) = \int I(t).V_g dt = Q_g V_g = en\frac{C_g}{C_\Sigma}V_g + \frac{C_t C_g V_g^2}{C_\Sigma}$$

To maintain electron number in quantum dot :

$$F(n) < F(n \pm 1) \Rightarrow [n - \frac{1}{2}]\frac{e}{C_g} < V_g < [n + \frac{1}{2}]\frac{e}{C_g}$$

Single-electron box

- Bias conditions ..

Free energy change in the transition of electron number from n to n +1:

$$\Delta F(n, n+1) = F(n+1) - F(n) = \frac{e}{C_t}(Q_t - Q_c)$$

$$\text{Where}: Q_c = \frac{e}{2}[1 + \frac{C_g}{C_t}]^{-1}$$

Single-electron transistor

- Schematic structure of a single-electron transistor (SET) is shown in the figure (fig 3)

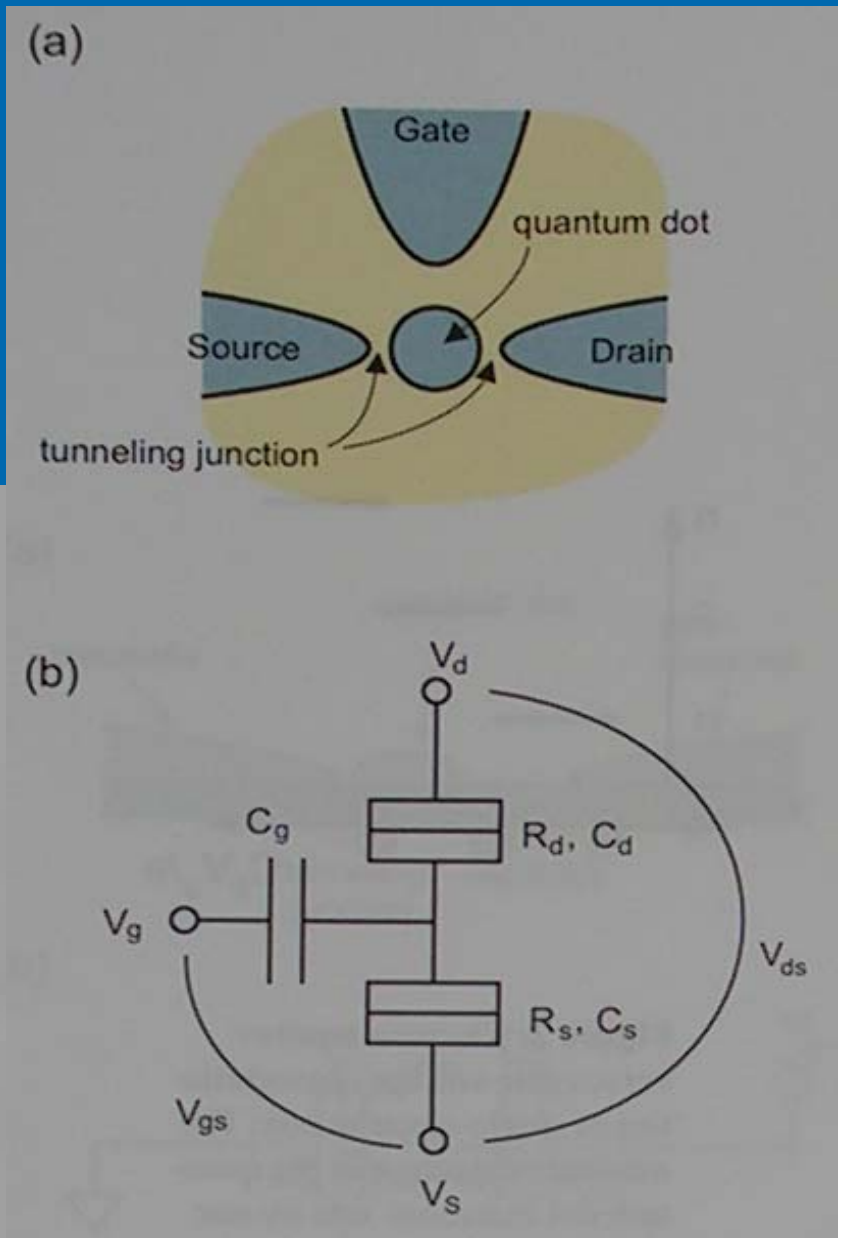


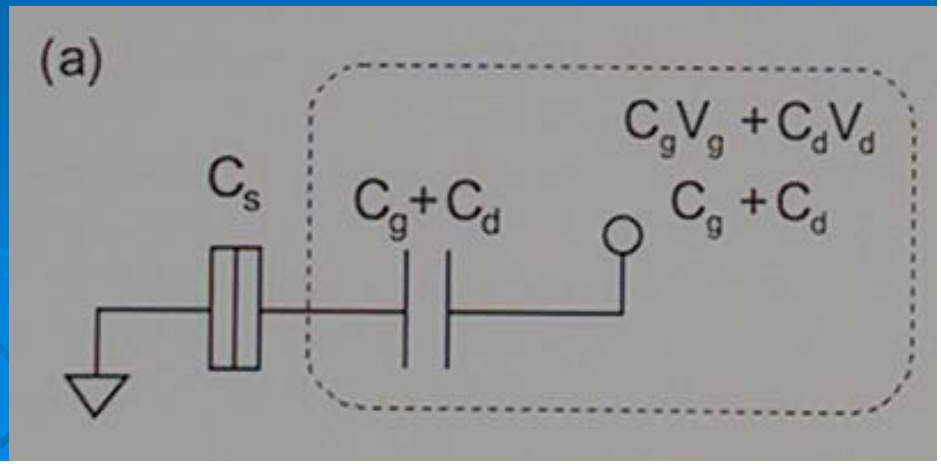
Figure 3:
(a) Schematic structure of single-electron transistor.
(b) Equivalent circuit of single-electron transistor.

Single-electron transistor

- Operation of a single-electron transistor
  - The circuit connected to the tunneling junction of source is shown in the figure (fig4a)
  - The condition for maintaining electron number at n is:

$$[n-\frac{1}{2}]\frac{e}{C_g+C_d}<\frac{C_gV_g+C_dV_d}{C_g+C_d}<[n+\frac{1}{2}]\frac{e}{C_g+C_d}\Rightarrow$$

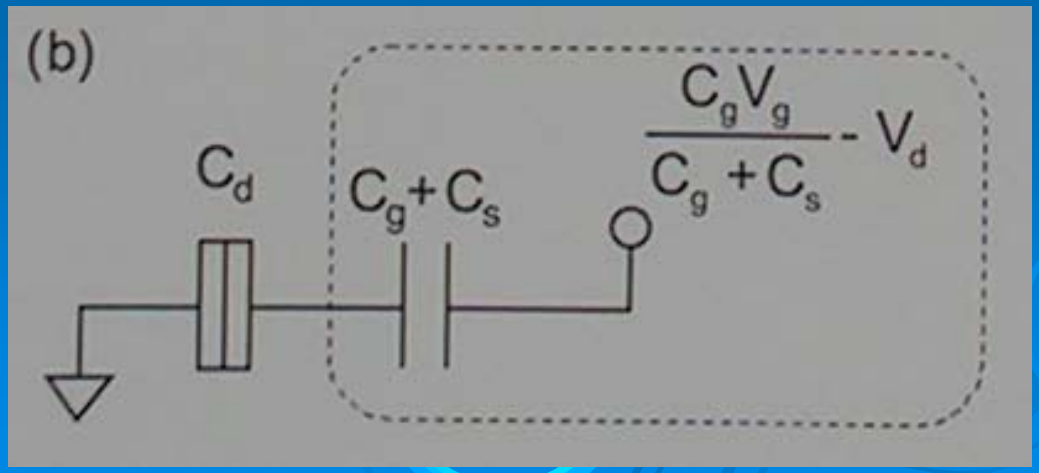
$$\frac{1}{C_d}[ne-\frac{e}{2}-C_gV_g]<V_d<\frac{1}{C_d}[ne+\frac{e}{2}-C_gV_g]$$



Single-electron transistor

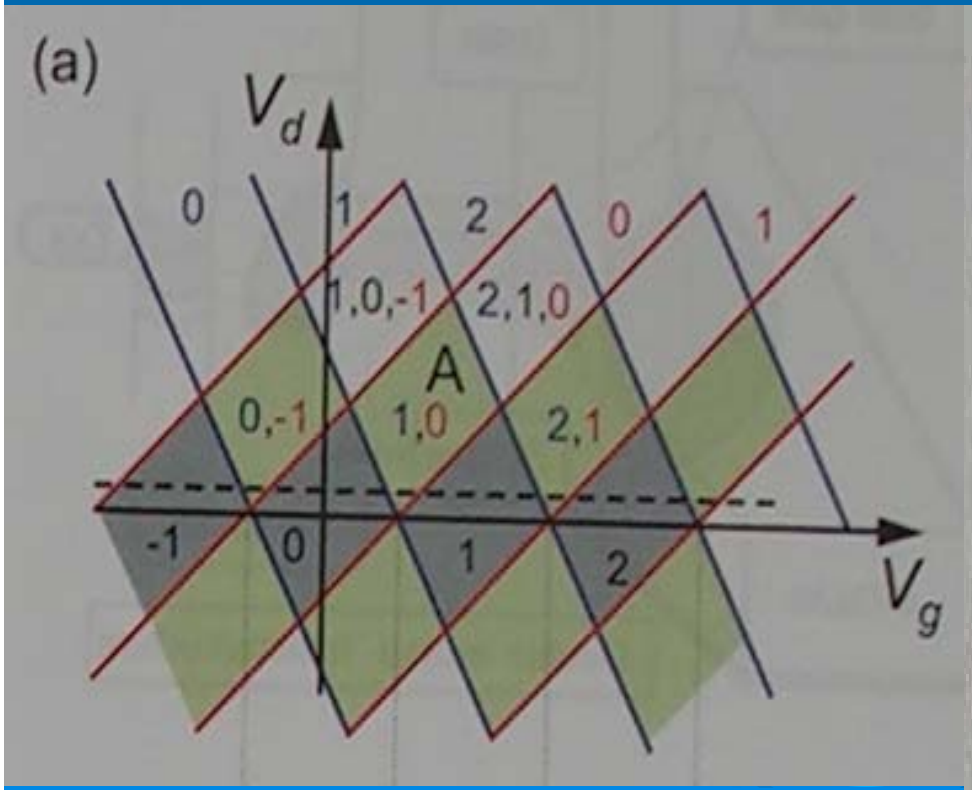
- The circuit connected to the tunneling junction of drain is transformed to the circuit shown in the figure (fig 4b)
- The condition to maintain the electron number at n is

$$\frac{1}{C_s + C_g}\left[-ne + \frac{e}{2} + C_g V_g\right] > V_d > \frac{1}{C_s + C_g}\left[-ne - \frac{e}{2} + C_g V_g\right]$$



Single-electron transistor

- Figure (fig 5a) shows the drain-gate voltage relation
- Gray areas are coulomb blockade areas where electron number in the dot is fixed



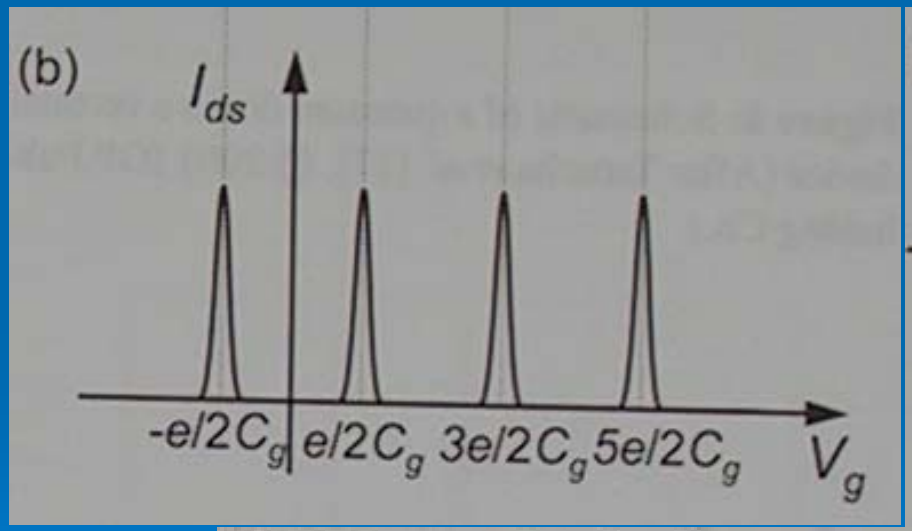
(a) Relationship between the drain voltage V_d and the gate voltage V_g, satisfying the conditions expressed by Eqs. (15) and (16). The diamond-shaped structure along the x-axis is called Coulomb diamond.

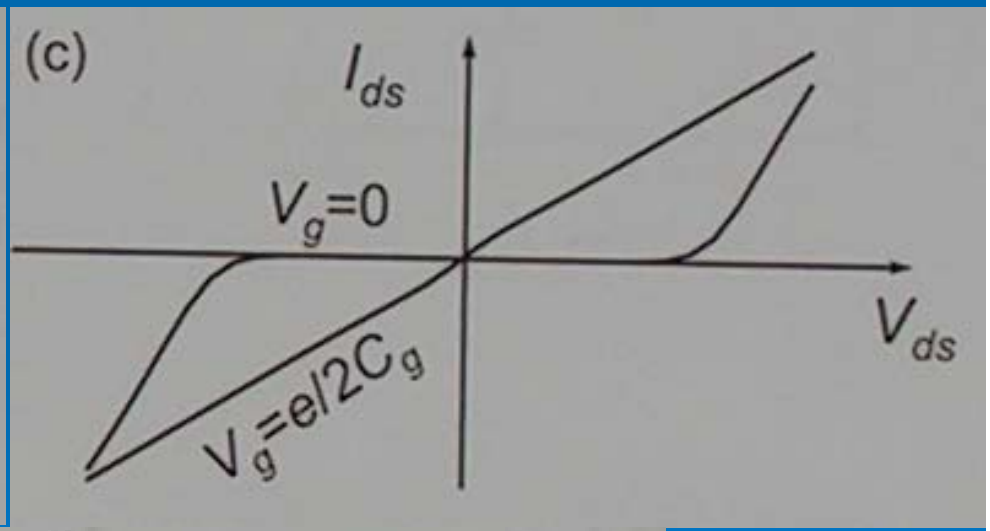
Single-electron transistor

- Green areas are regions with two preferable electron numbers (one for source and one for drain)
- In area labeled A:
  - Preferable electron number for source is 1 and for drain is 0
  - Electron tunnels from source to dot to make its electron number 1
  - Then it tunnels from dot to drain to change the electron number of the dot to 0

Single-electron transistor

- Figure (fig 5b) shows the oscillating I_{ds} versus V_g characteristic of the SETs
- Typical I_{ds} versus V_{ds} characteristics are shown in figure (fig 5c)





(b) source-to-drain current I_{ds} versus gate voltage V_g characteristics of single-electron transistors. (c) I_{ds} versus V_{ds} characteristics of single-electron transistors.

Single-electron transistor

- Figure (fig 6) demonstrates a implementation of a circular disk quantum dot sandwiched between source and drain and surrounding gate

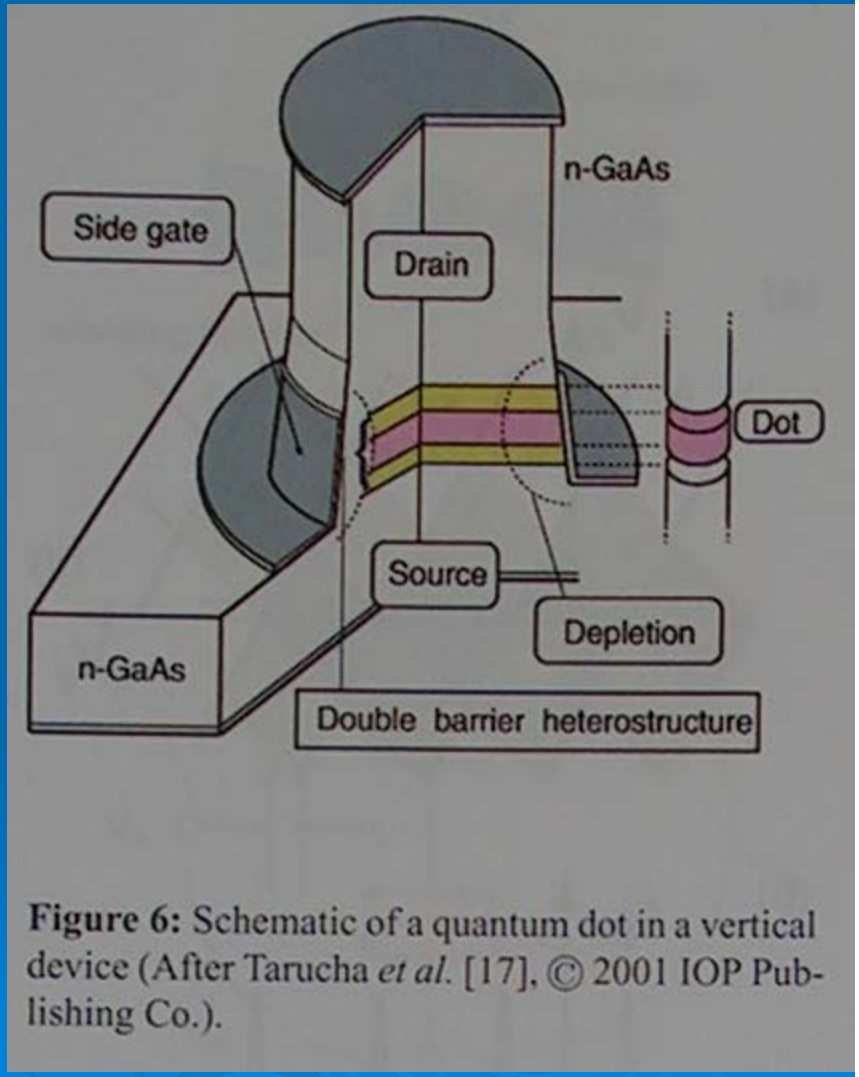


Figure 6: Schematic of a quantum dot in a vertical device (After Tarucha *et al.* [17], © 2001 IOP Publishing Co.).

Single-electron transistor

- Figure (fig 7) shows Ids-Vg characteristics of the fabricated SET, inset of the figure is the electron addition energies and part b shows the energy required for adding electrons

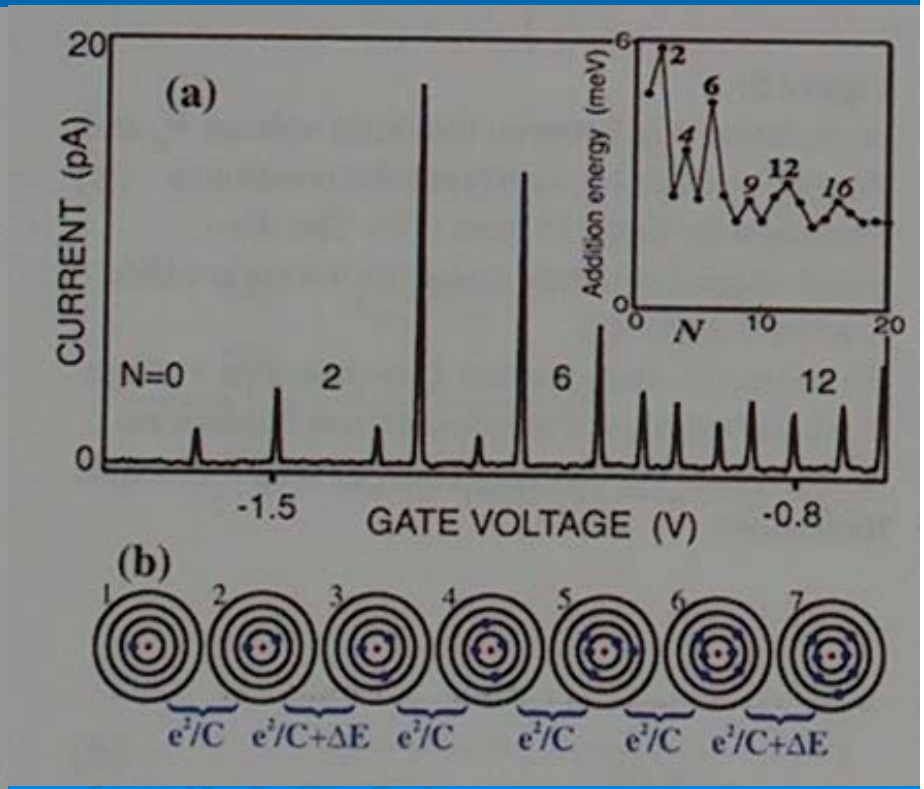


Figure 7: Current flowing through a two dimensional circular quantum dot on varying the gate voltage.
(a) The first peak marks the voltage where the first electron enters the dot, and the number of electrons, *N*, increases by one at each subsequent peak. The distance between adjacent peaks corresponds to the addition energies (see inset).
(b) The addition of electrons to circular orbits is shown schematically. The first shell can hold two electrons whereas the second shell can contain up to four electrons. It therefore costs extra energy to add the third and seventh electrons (After Kouwenhoven *et al.* [16], © 2001 IOP Publishing Co.).

Single-electron transistor

- Advantages and disadvantages of SETs compared to MOSFETs
  - SETs:
    - low power consumption
    - Good scalability
    - Operation of SETs is limited to low temperatures
    - High output impedance (Rt must be much higher than 25.8 kOhms)
    - Source-drain voltage of the SETs must be smaller than the gate swing voltage
  - For room temperature operation, dot must be much smaller than 10 nm, fabrication of a 10 nm structure is difficult in current technology

Other Single Electron Devices

- Other single electron devices
  - Single electron turnstile and single electron pump are devices that can control timing of single electron tunneling
- Fabrication of single electron devices
  - Single electron devices have been fabricated in a variety of materials such as aluminum, hetrostructures and silicon
  - Fabrication on silicon is done by fine-lithography or by growth of silicon dots by deposition process

Application of single electron devices to logic circuits

- Introduction
  - Many attempts have been made to develop logic circuits consisting of single electron devices
  - Two approaches in logic applications:
    - Representing a bit by a single electron and using single electron devices to transfer electrons one by one
    - Representing a bit by more than a single electron and using single electron devices to switch the current on/off
  - Former uses less power, latter results in more operation stability

Application of single electron devices to logic circuits

- Analytical model of SET for circuit simulation
  - Assumptions
    - Source and drain of the SETs are connected to capacitors much larger than total capacitance of the SET island or biased by constant voltage sources
    - Source and drain resistances are assumed to be the same (Rs=Rd=Rt)
    - At each given gate voltage, the two most probable numbers of electrons in the SET island are taken into account
    - Tunneling resistance is supposed to be much larger than quantum of resistance h/e^2~25.8kOhms

Application of single electron devices to logic circuits

- Derivation of the model
  - I-V characteristics of SET having n or n+1 electrons is given by

$$I_n = \frac{e}{2R_\Sigma C_\Sigma} \frac{(\tilde{V}_{gs,n}{}^2 - \tilde{V}_{ds}{}^2)\sinh(\tilde{V}_{ds}/\tilde{T})}{V_{gs,n}\sinh(\tilde{V}_{gs}/\tilde{T}) - \tilde{V}_{ds}\sinh(\tilde{V}_{ds}/\tilde{T})}$$

where

$$\tilde{V}_{gs,n} = \frac{2C_g V_g}{e} - \frac{(C_g + C_s - C_d).V_{ds}}{e} - 1 - 2n,$$

$$\tilde{V}_{ds} = \frac{C_\Sigma V_{ds}}{e},\ \tilde{T} = \frac{2k_B T C_\Sigma}{e^2},\ R_\Sigma = R_t + R_t\,(R_t = R_s = R_d)$$

Application of single electron devices to logic circuits

- It corresponds to one period of Coulomb oscillations
- Gate voltage giving peak of Coulomb oscillations is:

$$V_{gs} = \frac{e}{2C_g} + \frac{ne}{C_g} + \frac{(C_g + C_s - C_d).V_{ds}}{2C_g}$$

- Considering the period of Coulomb oscillations e/Cg, gate voltage range is obtained as

$$\frac{ne}{C_g} + \frac{(C_g + C_s - C_d).V_{ds}}{2C_g} < V_{gs} < \frac{(n+1)e}{C_g} + \frac{(C_g + C_s - C_d).V_{ds}}{2C_g}$$

Application of single electron devices to logic circuits

- Figure (fig 13) shows coulomb oscillations over gate voltage range

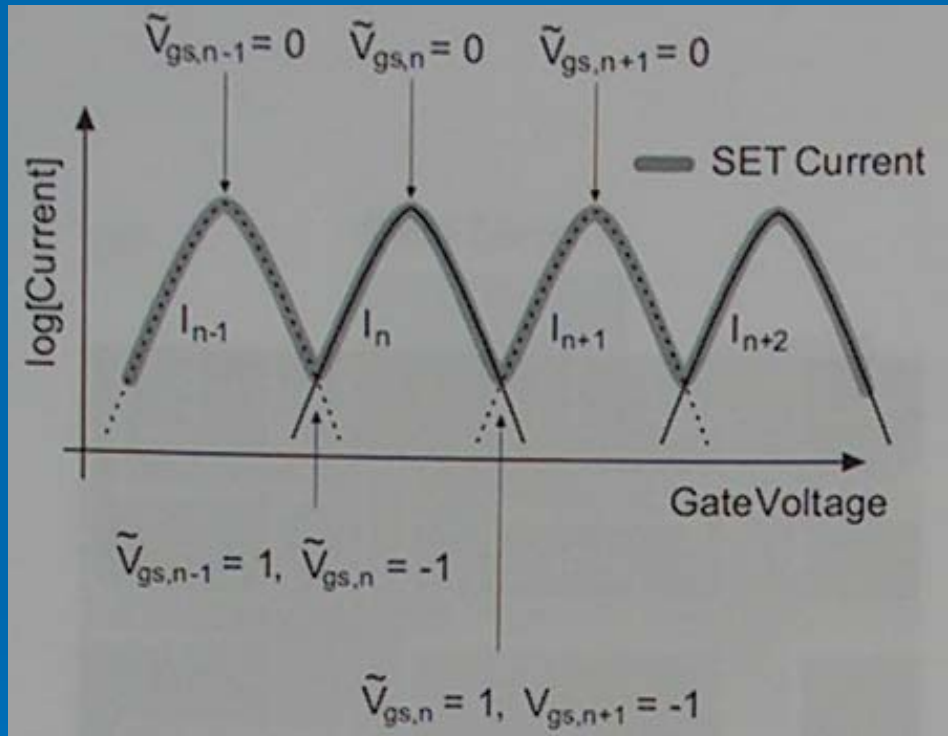


Figure 13: Schematic of model current I_{n-1}, I_n, ... , I_{n+2} (solid and dotted lines) and SET current (thick gray line). I_n defines one period of Coulomb oscillations. The summation of I_n over a desired gate voltage range gives the Coulomb oscillations.

Application of single electron devices to logic circuits

- Figure (fig 14) shows the Id-Vgs characteristics for a SET having C_s=C_d=1 aF, Cg=3 aF and R_t=10 MΩ

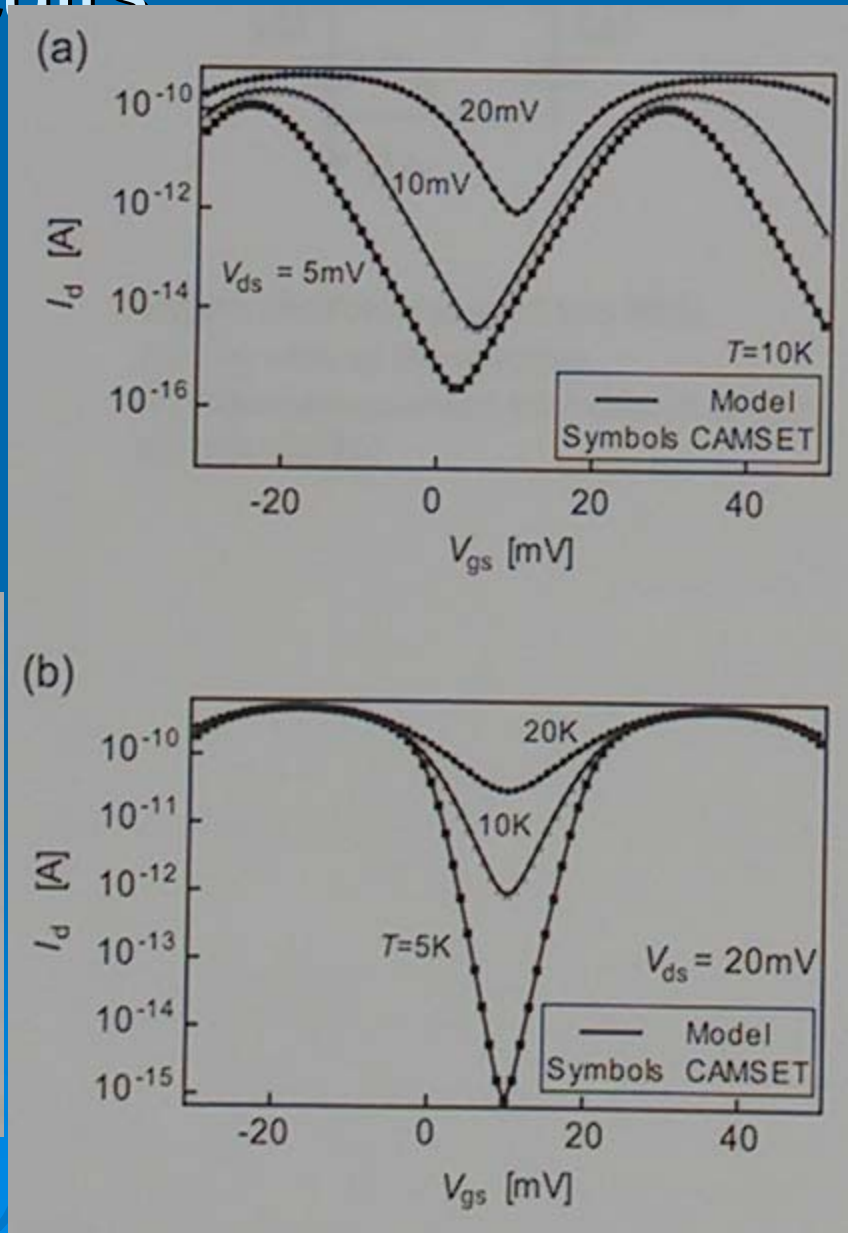
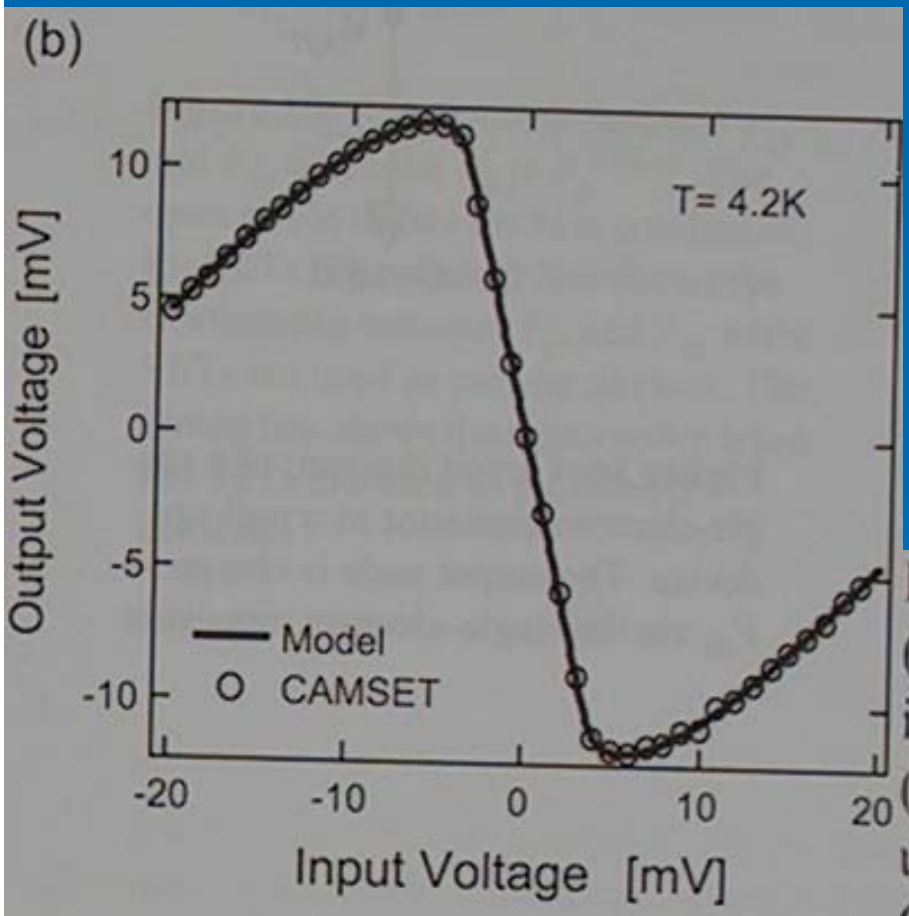


Figure 14: I_d - V_{gs} characteristics of a single-electron transistor, calculated using the SET model $I_{-1}+I_0$ (lines) and the reference simulator CAMSET (symbols) for various source-to-drain voltages (a) and temperatures (b). Here, C_g = 3 aF, C_s = C_d = 1 aF, R_t = 10 MΩ.

Application of single electron devices to logic circuits

- Figure (fig 15) shows a SET inverter
- Simulations are performed using SPICE



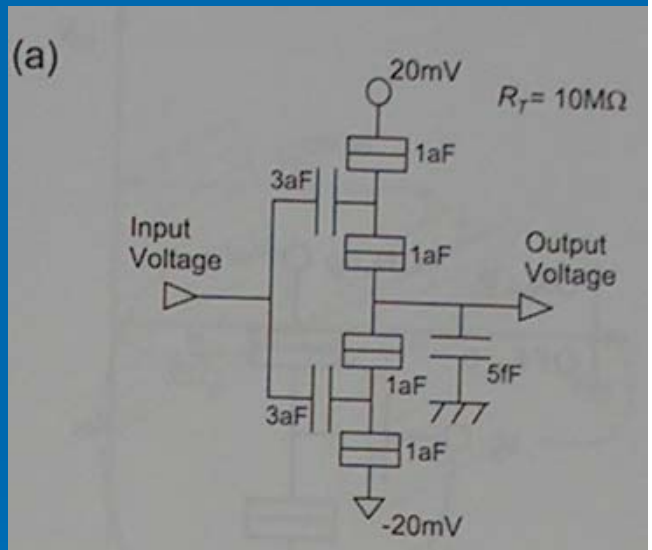
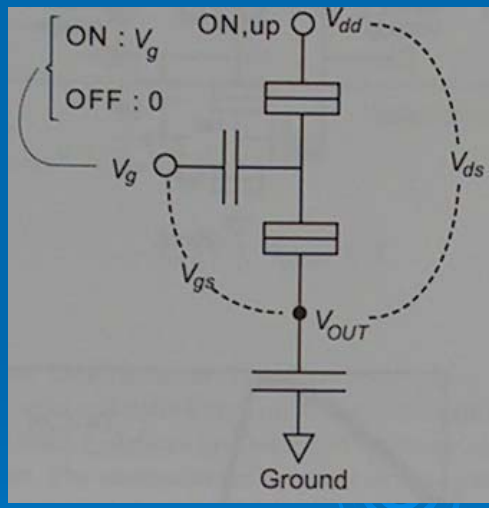


Figure 15:
(a) Schematic of a single-electron-transistor inverter.
(b) Characteristics of the SET inverter, calculated using the SET model (line) and the simulator CAMSET (symbols) at $T = 4.2$ K.

Application of single electron devices to logic circuits

- Logic circuits with single-electron transistors
  - Bias conditions for SETs (to turn SETs on)
    - Figure (fig 16) shows a SET circuit where the SET is used as a pull up device



$$V_{ds} = V_{dd} - V_{OUT},\ V_{gs} = V_g^{ON,up} - V_{OUT}$$

$$V_{gs} = V_g^{ON,up} - V_{dd} + V_{ds}$$

SETs must be turned on even at a source - drain voltage around zero, hence :

$$V_{gs} = \frac{e}{C_g}[\frac{1}{2} + n] \text{ at } V_{ds} = 0 \Rightarrow V_g^{ON,up} = V_{dd} + \frac{e}{C_g}[\frac{1}{2} + n]$$

$$V_{gs} = V_{ds} + \frac{e}{C_g}[\frac{1}{2} + n]$$

Application of single electron devices to logic circuits

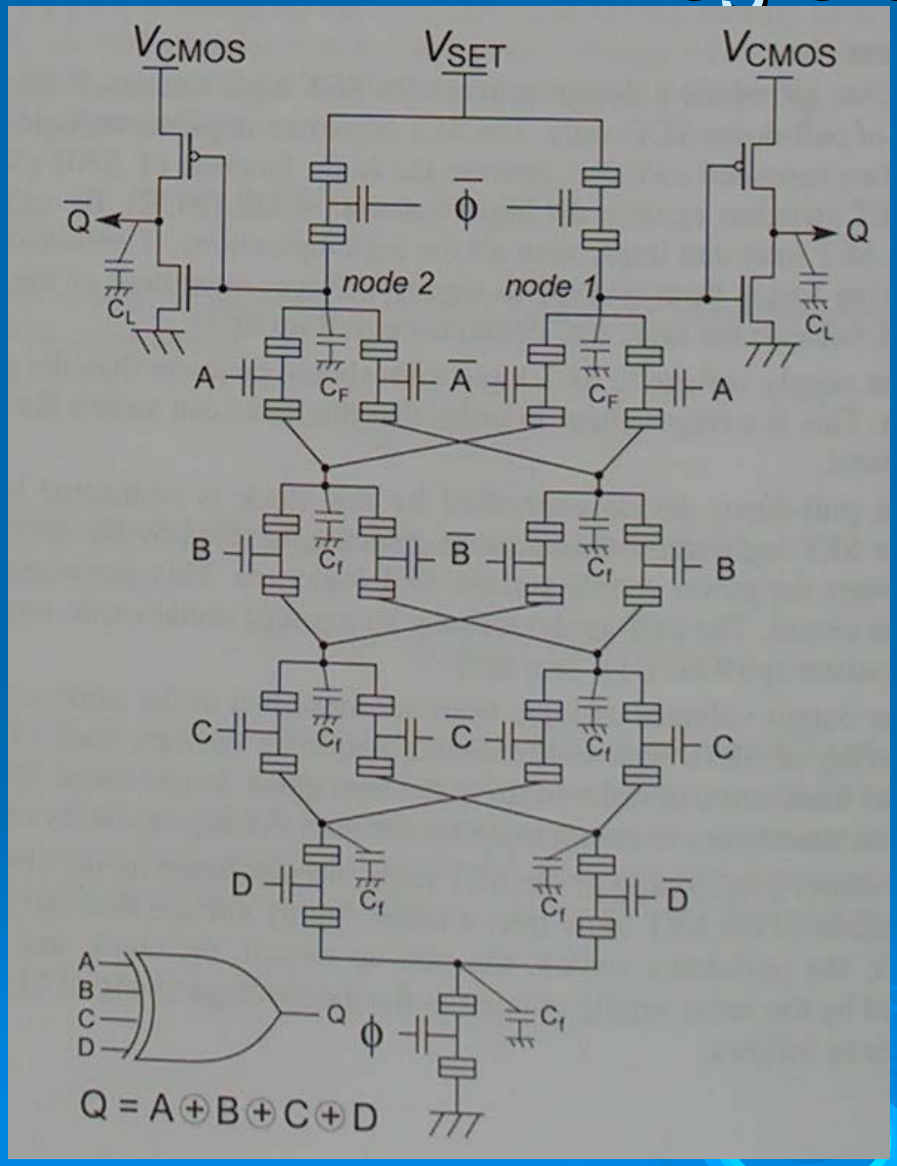
- Conditions to turn SETs off

$$\text{at } V_{gs} = 0,\ V_{ds} \text{ is required to be :}$$

$$-\frac{e}{2(C_g + C_s)} < V_{ds} < \frac{e}{2(C_g + C_s)}$$

- Design scheme
  - Figure (fig 19) is a schematic of SET logic circuits
  - SET logic tree consists of pull-down SETs only
  - Clock Low: precharge period, load capacitor is charged regardless of inputs of SETs
  - Clock High: Evaluation period, pull-down device is turned on, logic state of the output will be determined depending on the inputs
  - (similar to CMOS dynamic logic)

Application of single electron devices to logic circuits



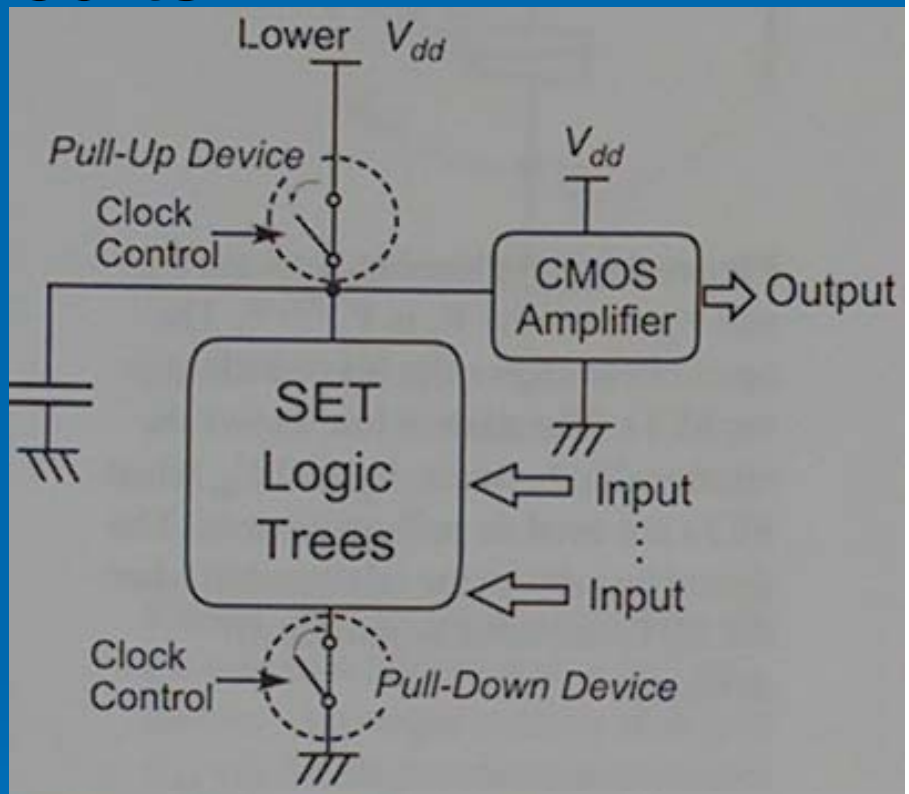


Figure 19: Schematic of SET logic circuits described in this section. The circuit consists of the SET logic tree, a lower supply voltage than the gate voltage swing of SETs, the pull-down switch, the pull-up switch, the clock, and the CMOS amplifier biased by the same voltage as the gate voltage swing of SETs.

Application of single electron devices to logic circuits

- Figure (fig 20) shows a 4-input XOR made with SETs
- Figure (fig 21) shows the simulation results

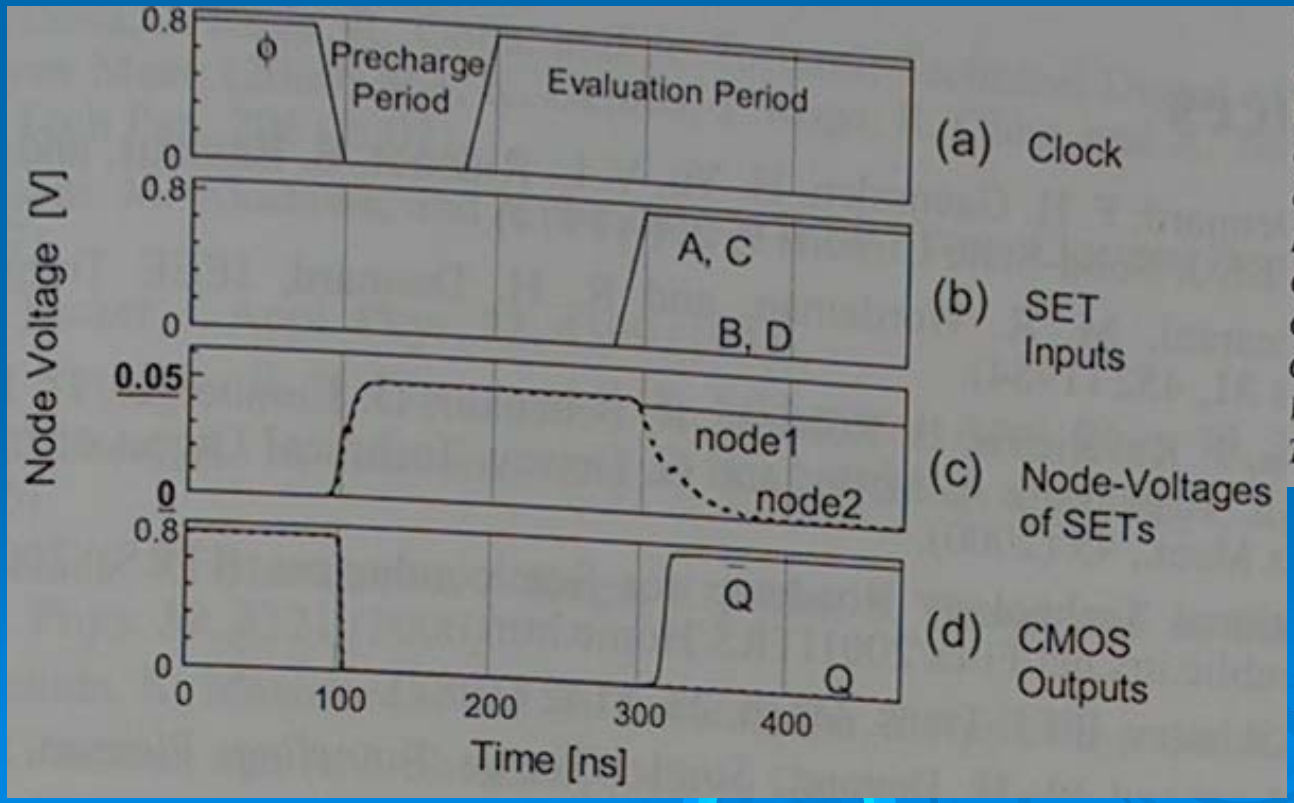


Figure 21: The simulated timing chart of the circuit shown in Figure 20. Here, $C_g = 0.1$ aF, $C_s = C_d = 0.06$ aF, $R_t = 500$ kΩ, $C_L = 10$ fF, $C_F = 1$fF, $C_f = 50$ aF, $V_{SET} = 50$ mV, and $T = 293$ K.