EE-612:
Lecture 25:
CMOS Circuits: Part 2

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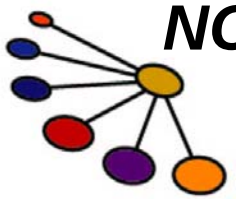
Fall 2006



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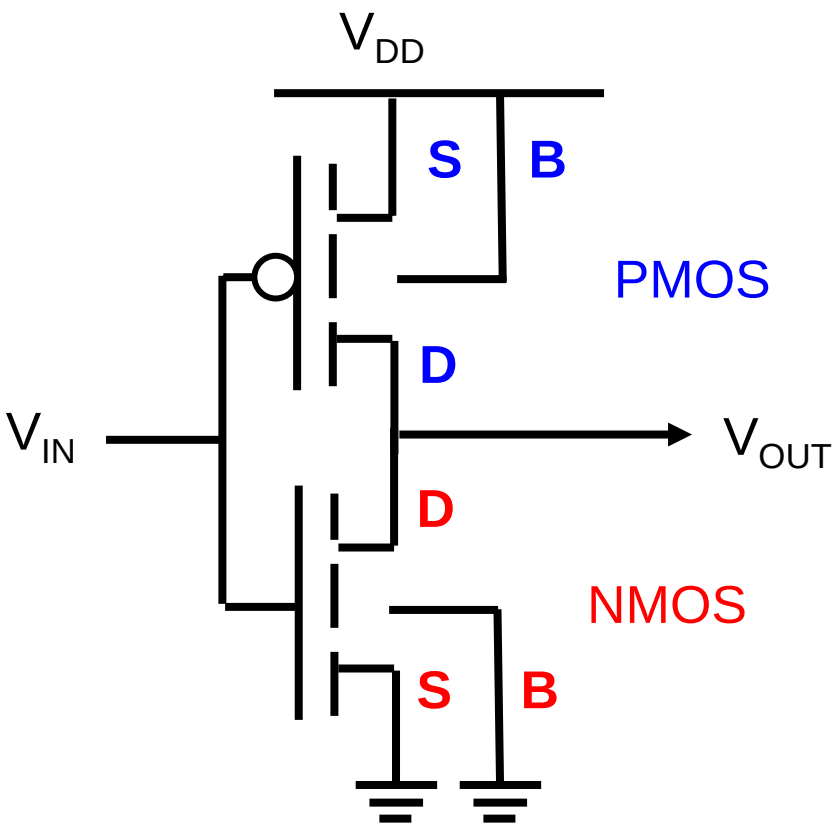
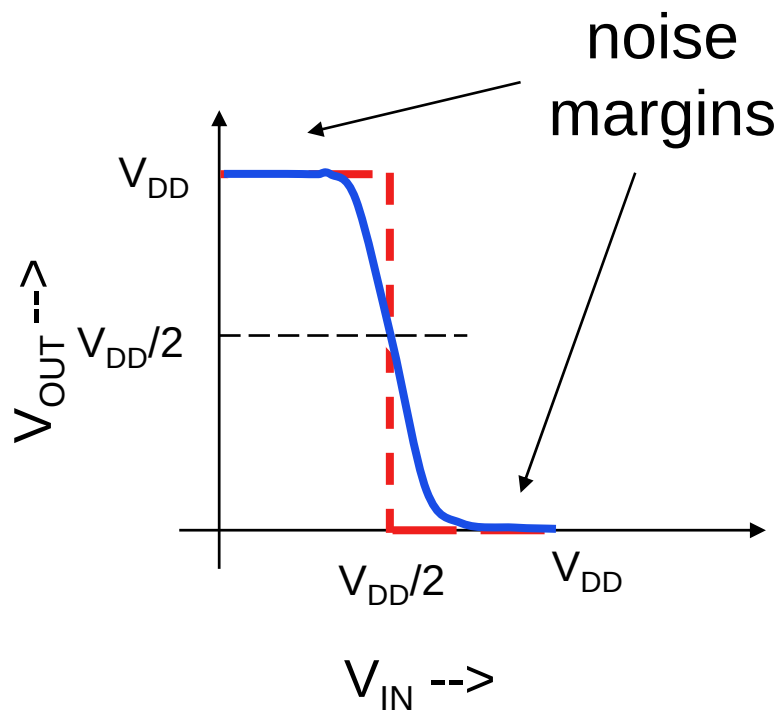
Outline

1) Review
2) Speed (continued)
3) Power
4) Circuit performance

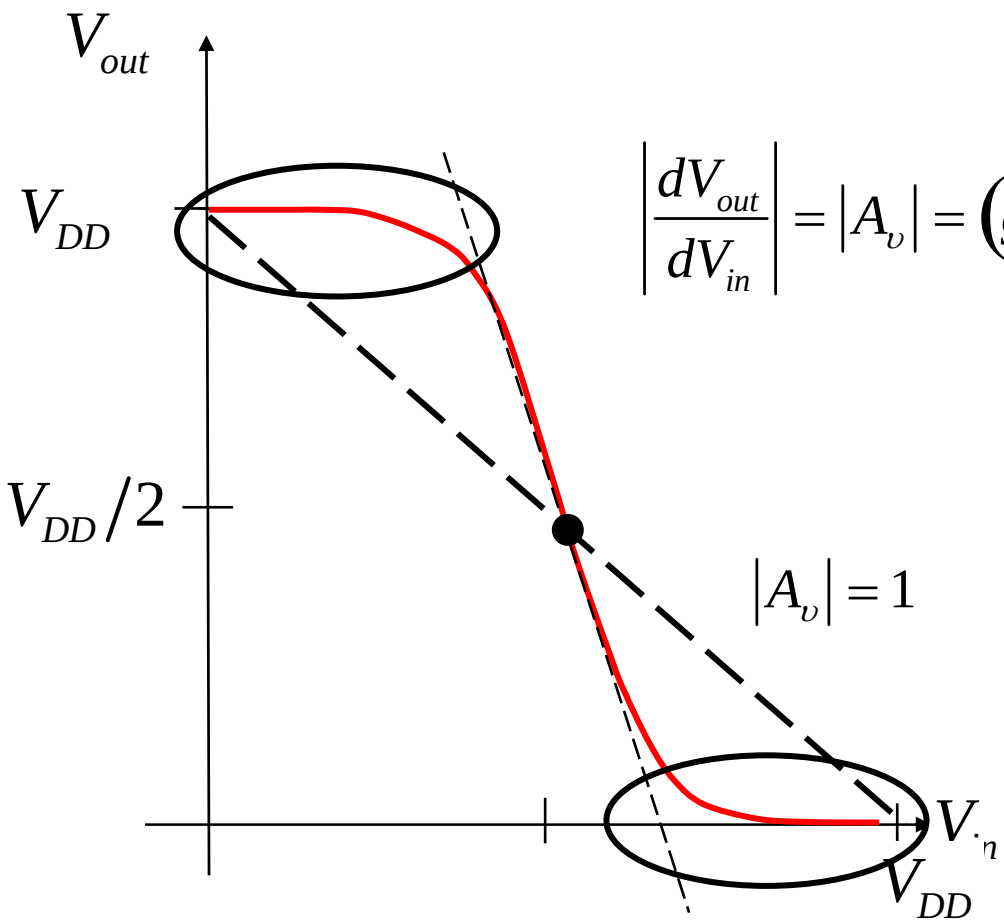
CMOS inverter



transfer characteristic



importance of gain



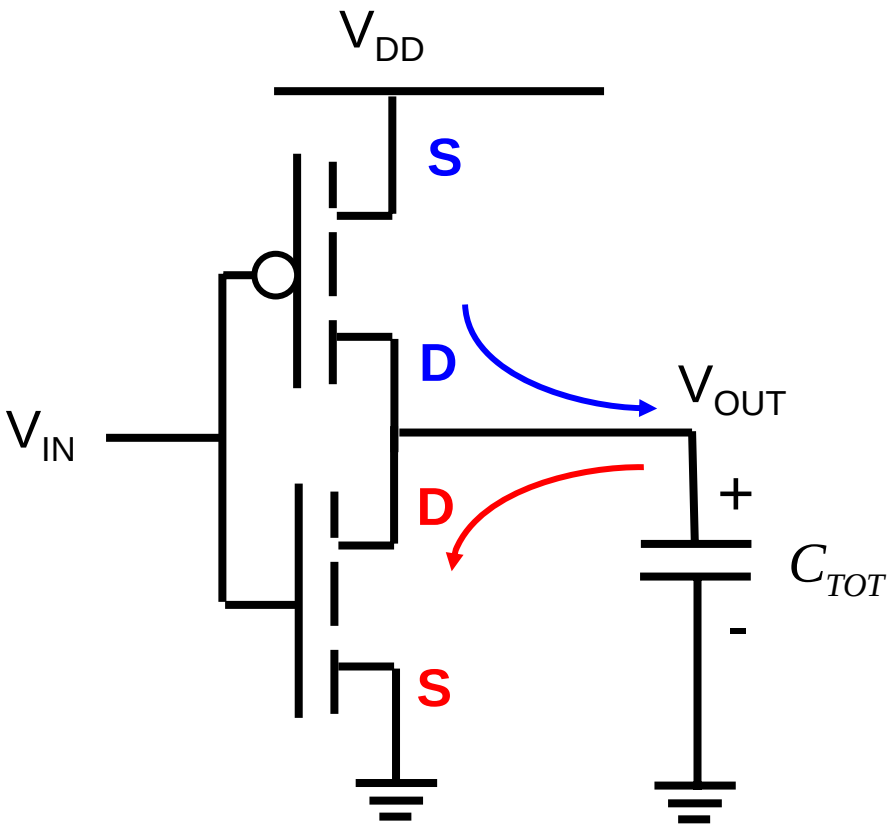
$$\left|\frac{dV_{out}}{dV_{in}}\right| = |A_\upsilon| = \left(g_{mn} + g_{mp}\right)\left(r_{on} \parallel r_{op}\right) > 1$$

must have gain to have noise margins

outline

1) Review
2) **Speed (continued)**
3) Power
4) Circuit performance

CMOS inverter speed



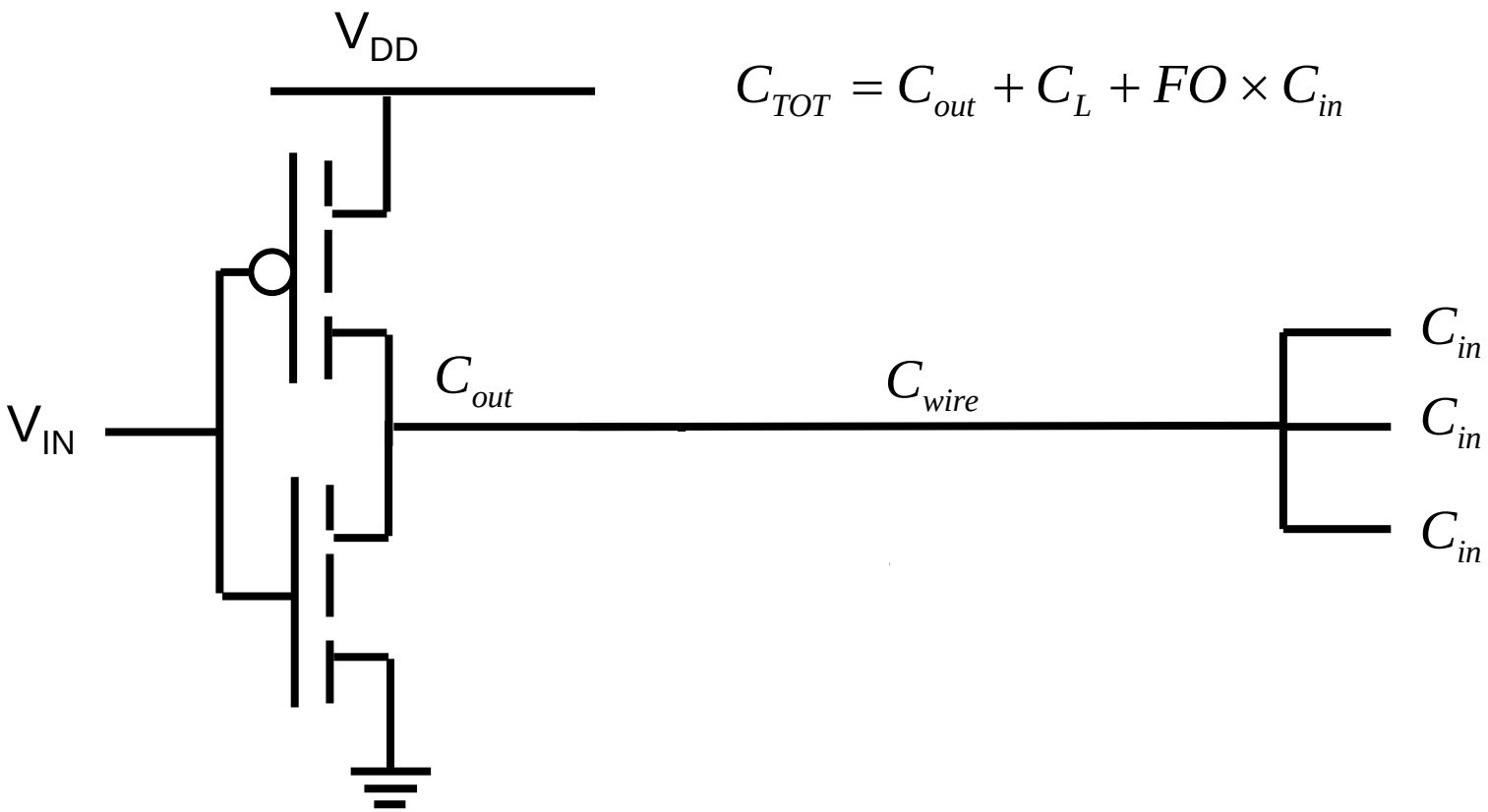
$$\tau = \frac{1}{2}\left(\frac{C_{TOT}V_{DD}}{2I_N(\text{on})} + \frac{C_{TOT}V_{DD}}{2I_P(\text{on})}\right)$$

$$\tau = \frac{\left(R_{swN} + R_{swP}\right)}{2}C_{TOT}$$

$$\tau = R_{sw}C_{TOT}$$

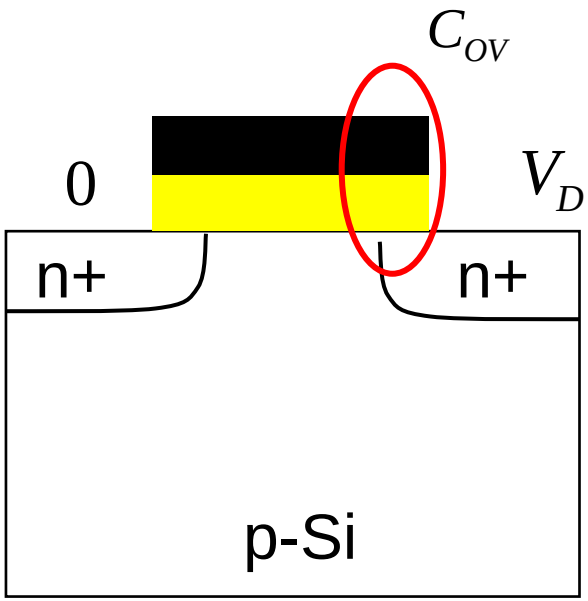
$$R_{swn} = k_n \frac{V_{DD}}{I_N(\text{on})} \qquad k_n > \frac{1}{2}$$

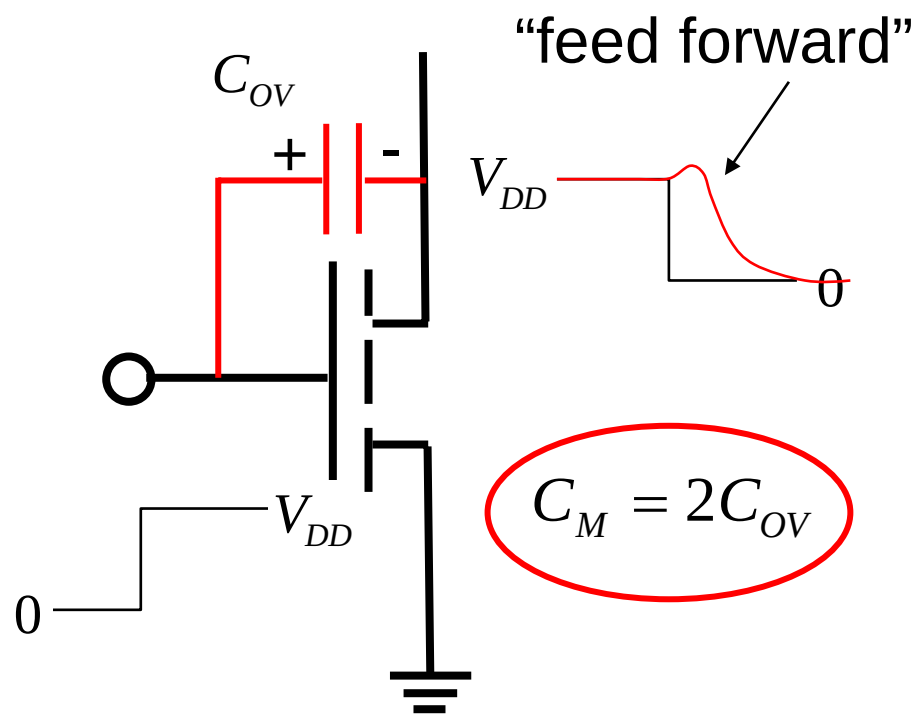
loaded propagation delay



$$C_{TOT} = C_{out} + C_L + FO \times C_{in}$$

Miller C





$$V_c(t << 0) = -V_{DD}$$

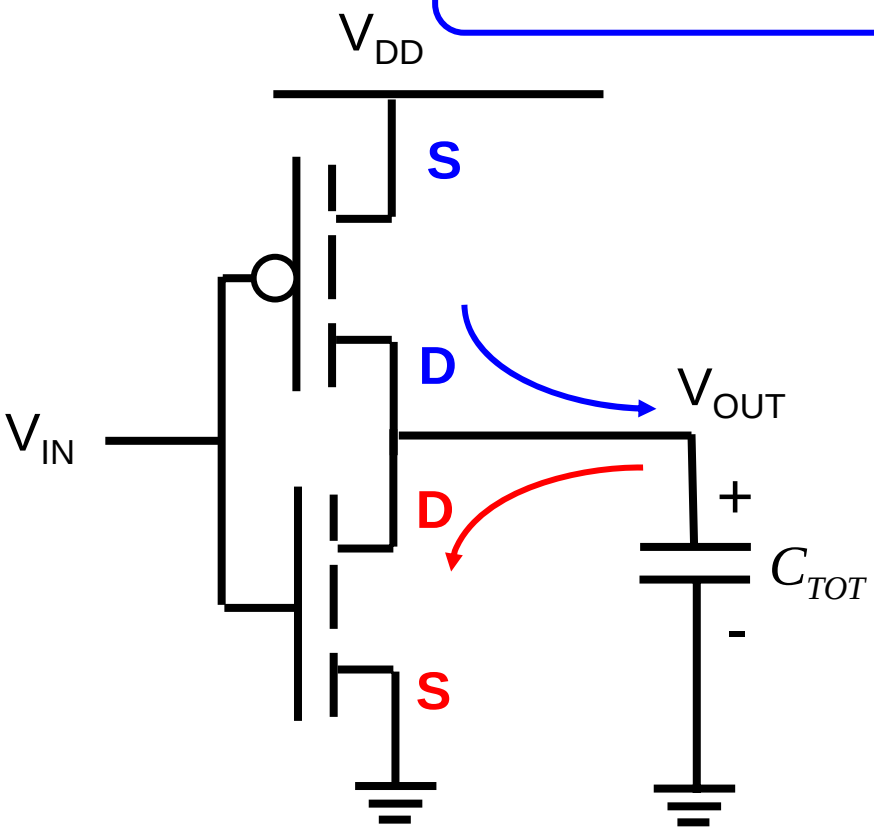
$$V_c(t >> 0) = +V_{DD}$$

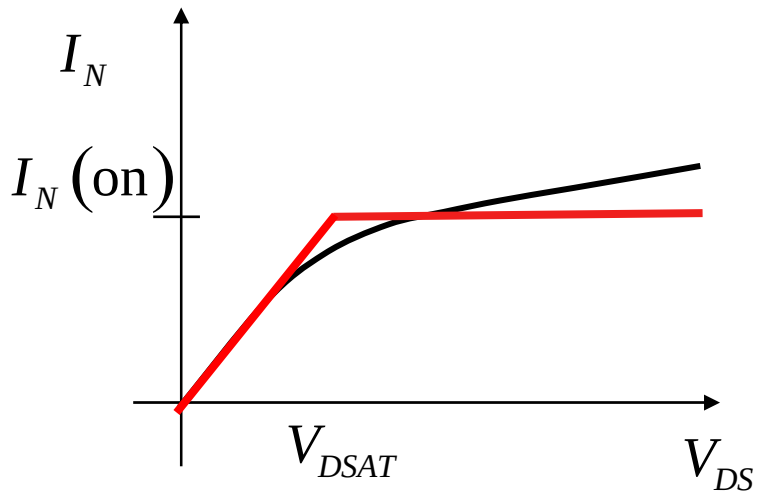
$$\Delta V_c = 2V_{DD}$$

$$\Delta Q_c = \Delta V_c C_{OV} = 2V_{DD}C_{OV} = C_M V_{DD}$$

on-current determines circuit speed

$$\tau = R_{sw} C_{TOT} \qquad R_{sw} \sim V_{DD} / I_D(\text{ON})$$





1) quasi-static assumption
2) simplified I_D - V_{DS}

metrics for circuit speed

K.K. Ng, et al., “Effective On-Current of MOSFETs for Large-Signal Speed Consideration,” IEDM, Dec., 2001.

M.H. Na, et al., “The Effective Drive Current in CMOS Inverters,” IEDM, Dec., 2002.

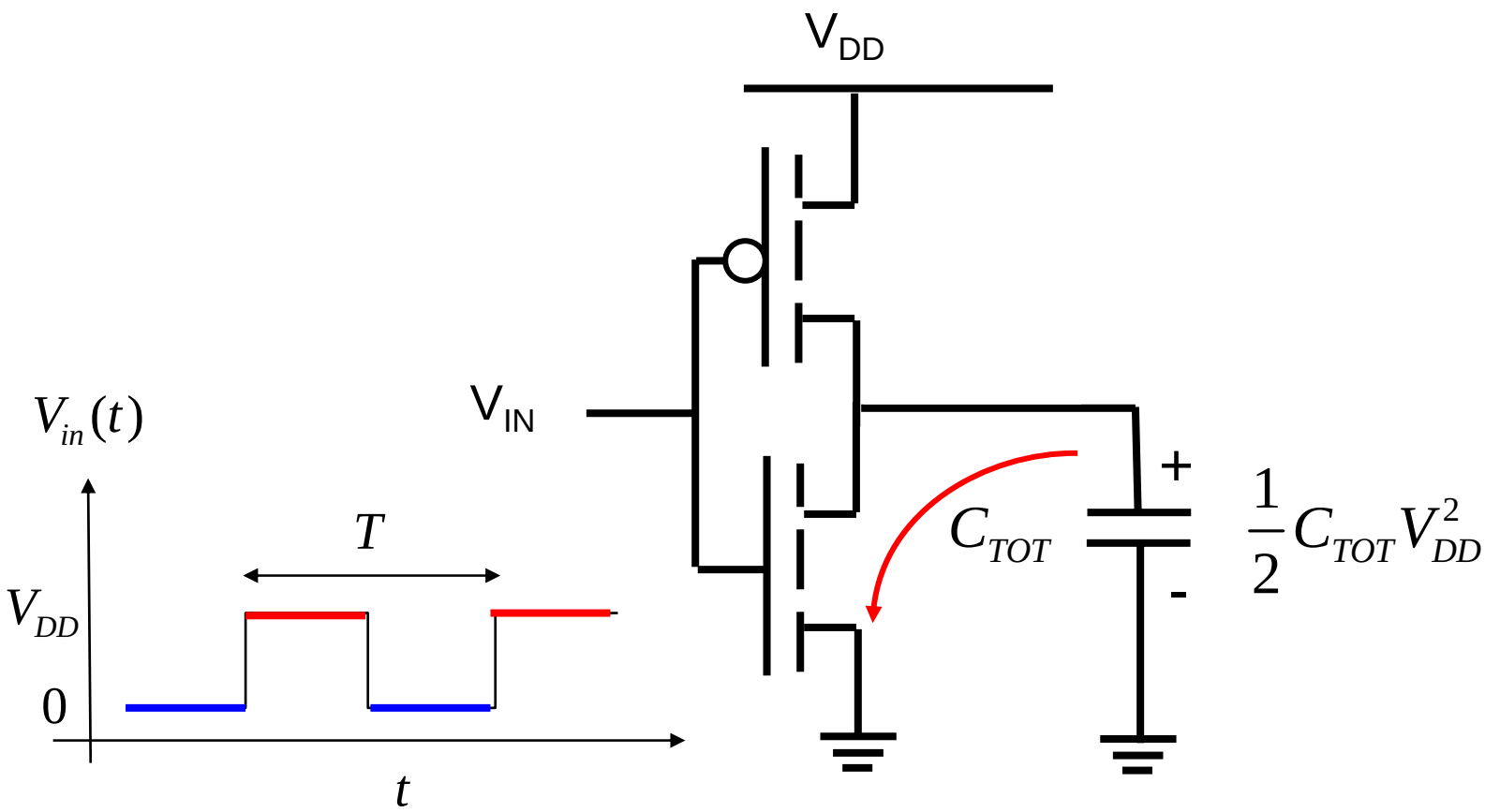
J. Deng and H.S.P. Wong, “Metrics for Performance Benchmarking of Nanoscale Si and Carbon Nanotube FETs Including Device Nonidealities,” *IEEE Trans. Electron Dev*., **53**, pp. 1317-1366, 2006.

R. Venugopal, et al., “Design of CMOS Transistors to Maximize Circuit FOM Using a Coupled Process and Mixed Mode Simulation Methodology,” *IEEE Electron Dev*. Lett., **53**, pp. 1317-1366, 2006.

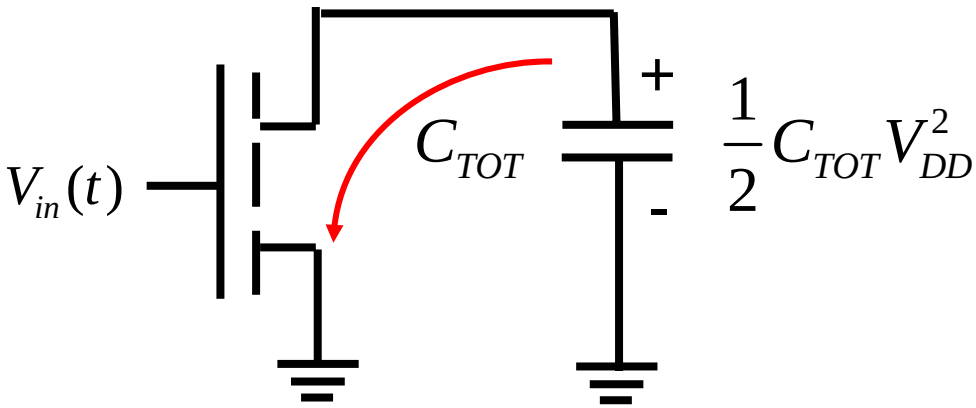
outline

1) Review
2) Speed
3) **Power**
4) Circuit performance

power



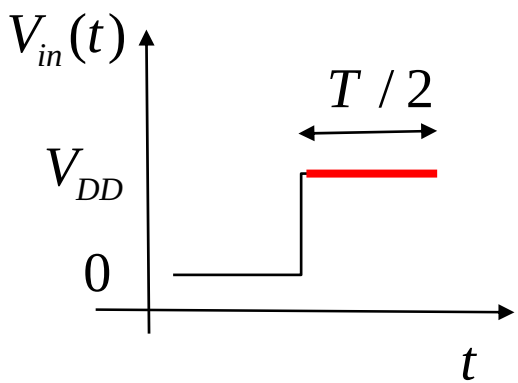
discharge cycle



$$E_C(0) = \frac{1}{2}C_{TOT}V_{DD}^2$$

$$E_C(T/2) = 0$$

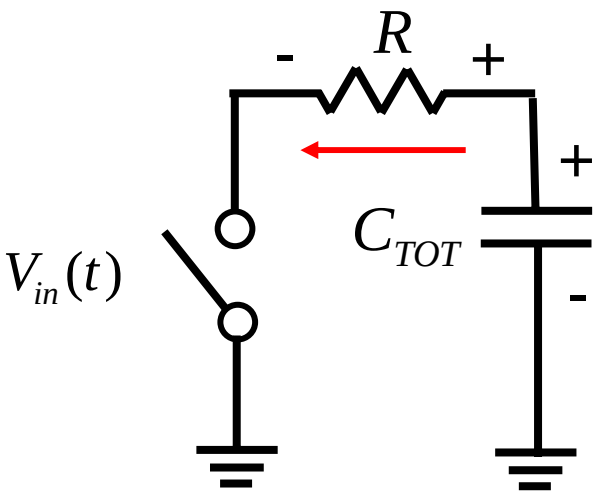
$$P_{dynamic} = \frac{\Delta E}{T/2} = \frac{C_{TOT}V_{DD}^2}{T}$$

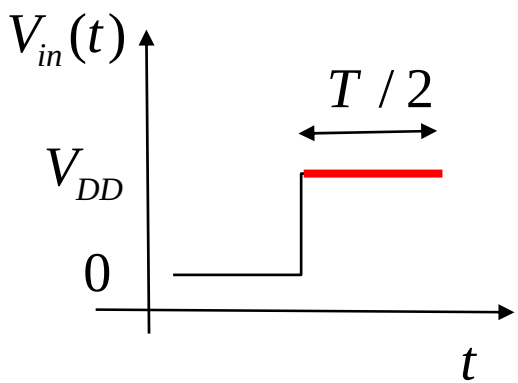


$$P_{dynamic} = \alpha f C_{TOT}V_{DD}^2$$

switching activity

discharge through a resistor





$$V_C(t) = V_c(0)e^{-t/RC_{TOT}} = V_{DD}\,e^{-t/\tau}$$

$$P_R(t) = V_C^2(t)/R$$

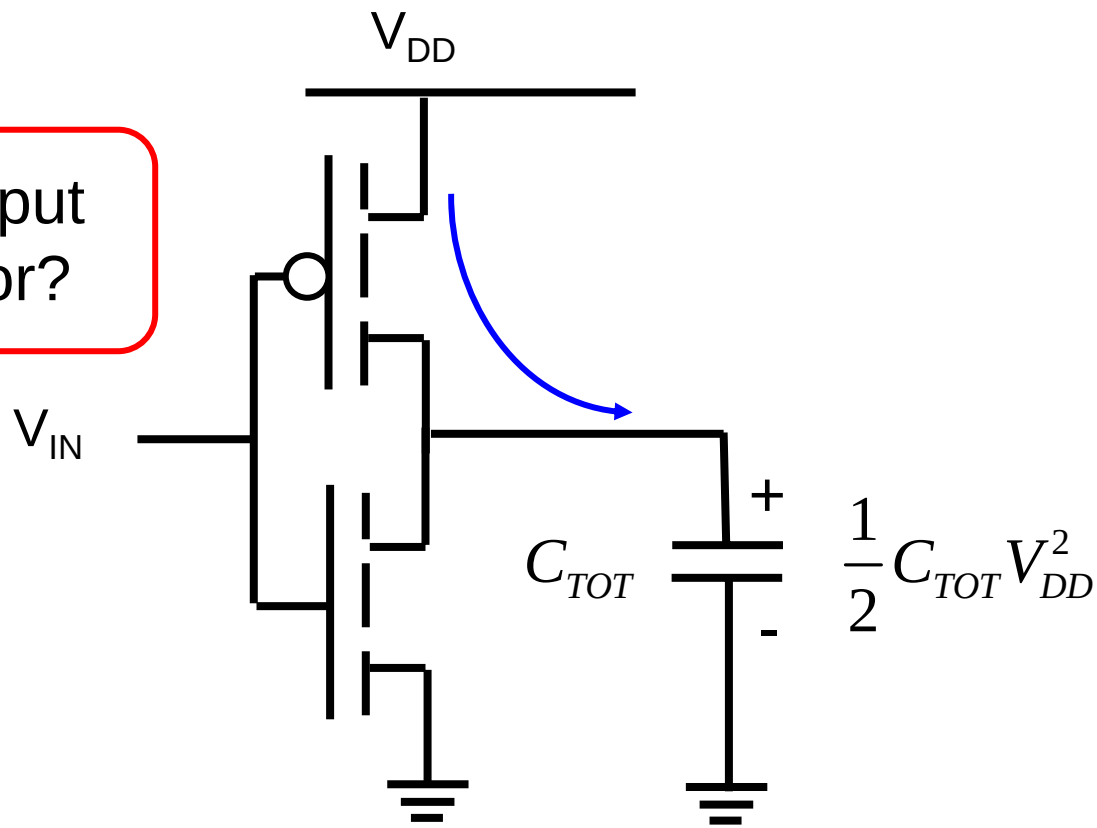
$$P_{AVE} = \frac{\int_0^{T/2} P_R(t)dt}{T/2}$$

$$= \frac{2}{T}\int_0^{T/2} \frac{V_{DD}^2}{R} e^{-2t/\tau}dt$$

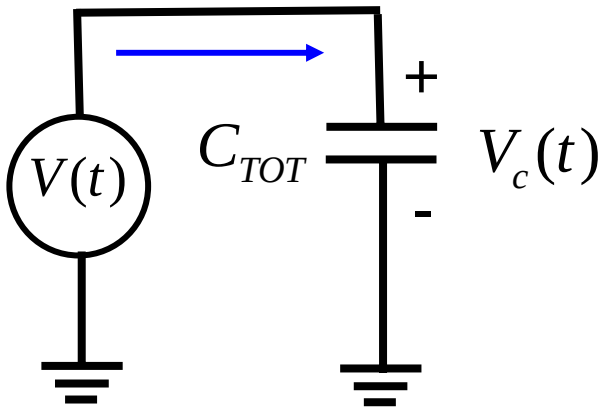
$$= f\,C_{TOT}V_{DD}^2$$

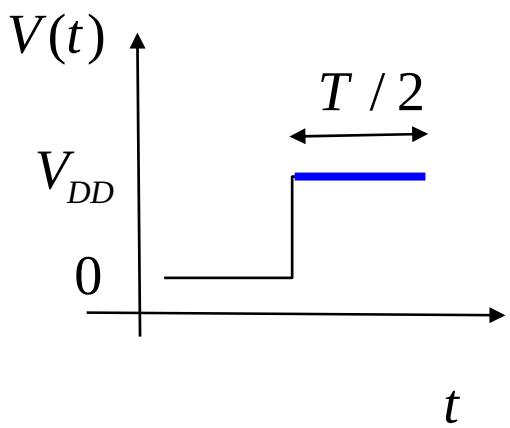
charging cycle

does it take power to put energy in the capacitor?



charging cycle (ii)





$$E_C(0) = 0$$

$$E_C(T/2) = \frac{1}{2} C_{TOT} V_{DD}^2$$

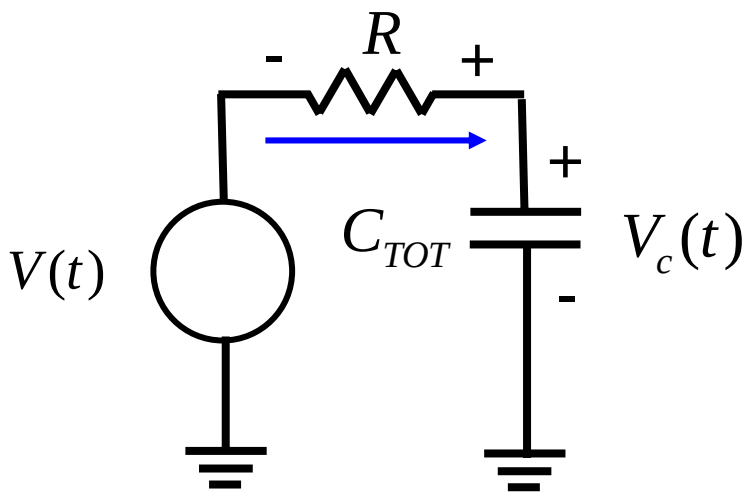
$$E_B = \int_0^{T/2} V_{DD} i(t) dt$$

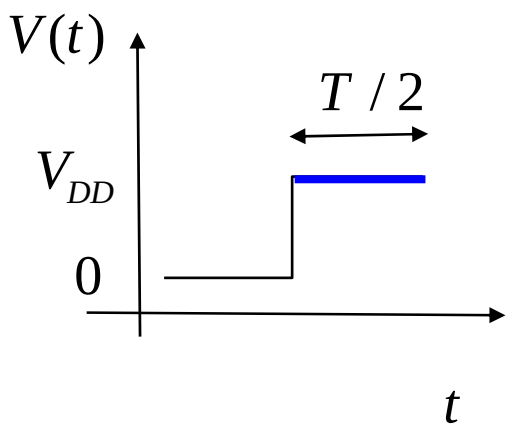
$$E_B = V_{DD} \int_0^{T/2} i(t)\, dt = V_{DD}\, Q$$

$$E_B = V_{DD} Q = C_{TOT} V_{DD}^2$$

$$E_{diss} = \frac{1}{2} C_{TOT} V_{DD}^2$$

charging cycle (iii)





$$i(t) = C_{TOT}\frac{dV_c}{dt}$$

$$V_c(t) = V_{DD} - i(t)R$$

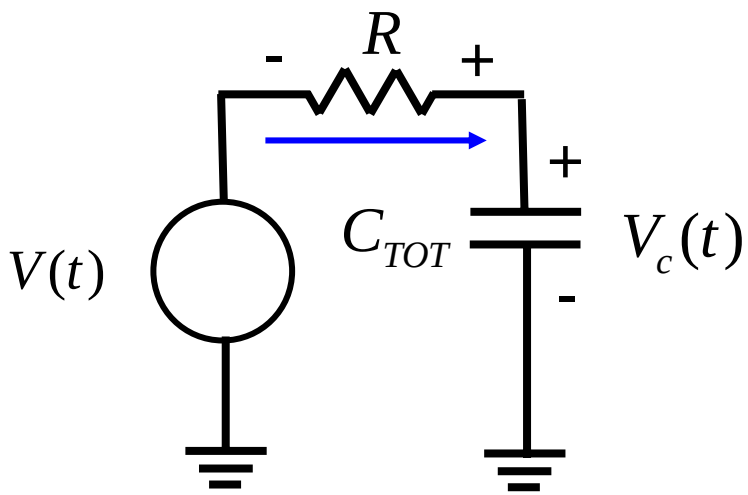
$$i(t) = -RC_{TOT}\frac{di}{dt}$$

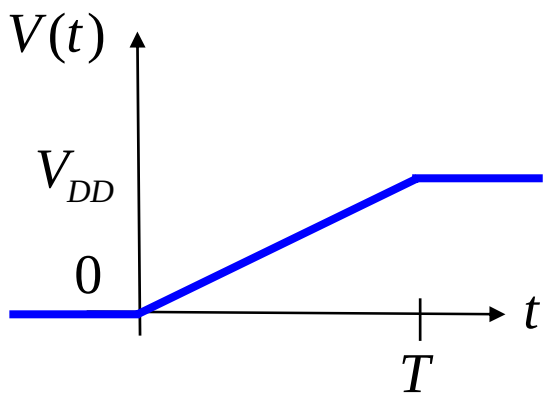
$$i(t) = i(0^+)e^{-t/\tau} = \left(V_{DD}/R\right)e^{-t/\tau}$$

$$E_B = \int_0^{T/2} V_{DD}\, i(t)\, dt = C_{TOT}V_{DD}^2$$

$$E_{diss} = \frac{1}{2}C_{TOT}V_{DD}^2$$

adiabatic charging





$$i(t) = C_{TOT}\frac{dV}{dt} = C_{TOT}\frac{V_{DD}}{T}$$

$$P_R = i^2 R = \left(\frac{C_{TOT}V_{DD}}{T}\right)^2 R$$

$$E_{diss} = \int_0^T P_R dt = \frac{C_{TOT}^2 V_{DD}^2}{T^2} RT$$

$$E_{diss} = C_{TOT}V_{DD}^2\left(\frac{RC_{TOT}}{T}\right)$$

outline

1) Review
2) Speed
3) Power
4) **Circuit performance**
5) CMOS circuit metrics

device impact on circuit performace

Question:

Given a technology, how does circuit performance depend on transistor design (W, T_{OX}, V_{DD}, etc.)

Taur and Ning assume a 250nm technology and explore this question by Spice simulation (see pp. 264 - 279). Can we understand the major trends simply?

effect of transistor *W* on delay

$$\tau = \frac{\left(R_{swn} + R_{swp}\right)}{2} C_{TOT} = R_{sw} C_{TOT}$$

$C_{TOT} = C_{out} + C_{wire} + FO \times C_{in}$	$R_{sw} = kV_{DD} / I_D(\text{on})$
$C_{out} \sim W$	$I(\text{on}) \sim W$
$C_{in} \sim W$	$R_{sw} \sim 1/W$

loaded vs. unloaded delay

$$\tau = R_{sw} C_{TOT} = R_{sw} \left(C_{out} + FO \times C_{in} + C_{wire} \right)$$

i) *unloaded:*
C_{in} and C_{out} dominate, $C_{TOT} \sim W$
--> τ ***independent of W***

ii) *loaded:*
C_L dominates, $C_{TOT} \sim$ *independent of W*
--> τ ***~1/ W***

effect of T_{OX} on delay

$$\tau = R_{sw} C_{TOT} = R_{sw} \left(C_{out} + FO \times C_{in} + C_L \right)$$

i) intrinsic delay (C_L = 0)

$$R_{sw} = kV_{DD} / I_D(\text{ON}) \sim T_{OX}$$
$$C_{in} \sim 1 / T_{OX}$$
$$C_{out} \quad \text{constant}$$

$$\Big\} \quad \tau_{\text{int}} \sim \text{constant}$$

ii) loaded delay (C_L > 0)

$$\tau_{loaded} \approx R_{sw} C_L$$

$$\Big\} \quad \tau_{loaded} \uparrow \quad \text{as} \quad T_{OX} \uparrow$$

(see Fig. 5.32 of Taur and Ning)

effect of *L* on delay

$$\tau = R_{sw} C_{TOT} = R_{sw}\left(C_{out} + FO \times C_{in} + C_L\right)$$

$$R_{sw} = kV_{DD} / I_D(\text{ON})$$

$$I_D(ON) = W C_{OX} \upsilon(0)\left(V_{GS} - V_T\right)\downarrow \quad \text{as} \quad L \uparrow$$

$$R_{sw} \uparrow \quad \text{as} \quad L \uparrow$$

$$C_{in} \sim L$$

$$C_{out}, C_L \quad \text{constant}$$

$$\Bigg\} \quad \tau \uparrow \quad \text{as} \quad L \uparrow$$

(see Fig. 5.31 of Taur and Ning)

effect of V_{DD} on delay

$$\tau = R_{sw} C_{TOT} = R_{sw}\left(C_{out} + FO \times C_{in} + C_L\right)$$

$$R_{sw} = kV_{DD} / I_D(\text{ON})$$

$$I_D(ON) = W C_{OX} \upsilon(0)\left(V_{GS} - V_T\right)$$

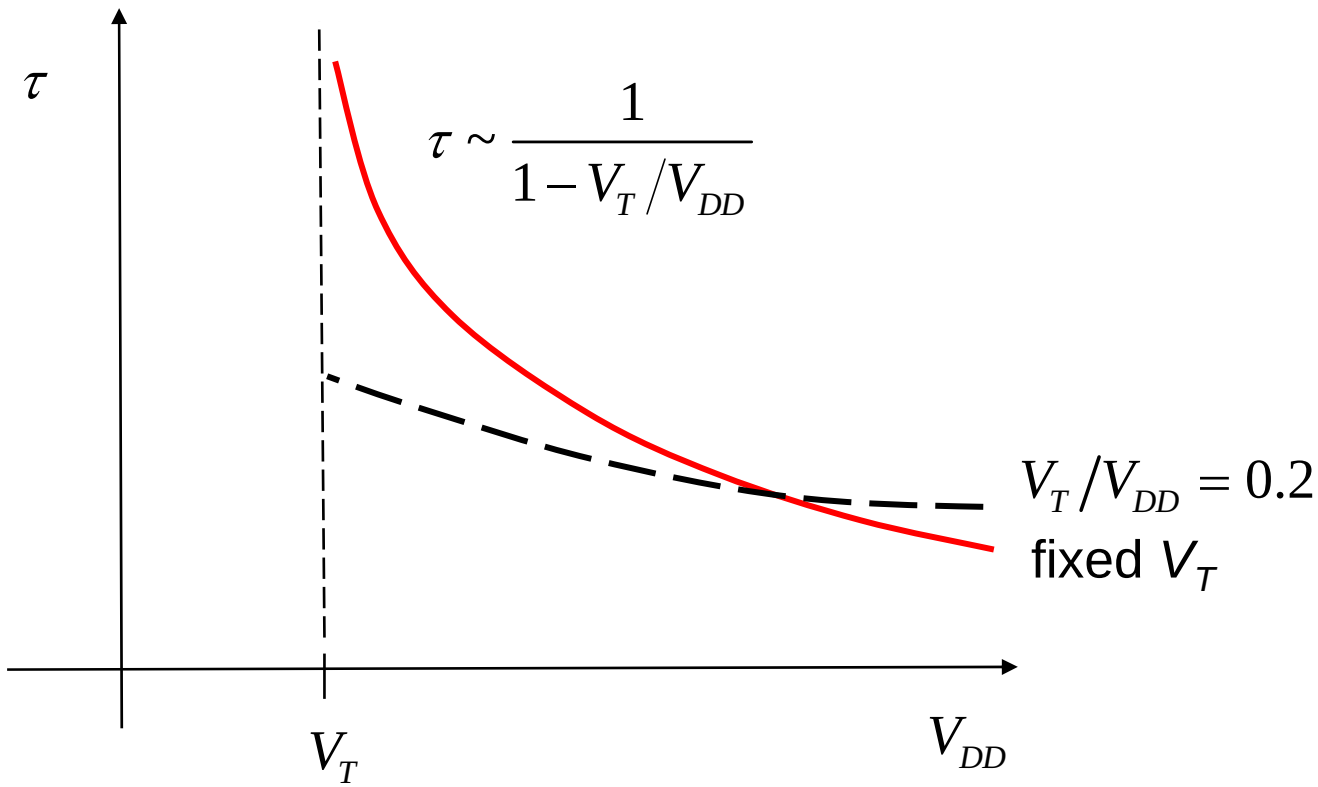
$$R_{sw} \sim V_{DD} \Big/ \left(V_{DD} - V_T\right)$$

$$R_{sw} \sim 1 \Big/ \left(1 - V_T / V_{DD}\right)$$

$$C_{out} = \varepsilon_{Si} / W_D \sim 1 \Big/ \sqrt{V_{DD} + V_{bi}}$$

$$\tau \sim \frac{1}{1 - V_T / V_{DD}}$$

delay vs. V_{DD}



$$I_D(\text{off}) \sim e^{-qV_T / mk_{BT}}$$

(see Fig. 5.33 of Taur and Ning)

power-delay trade-off

circuit speed:

$$\tau \sim V_{DD}/(V_{DD} - V_T) \qquad f \sim (1 - V_T/V_{DD})$$

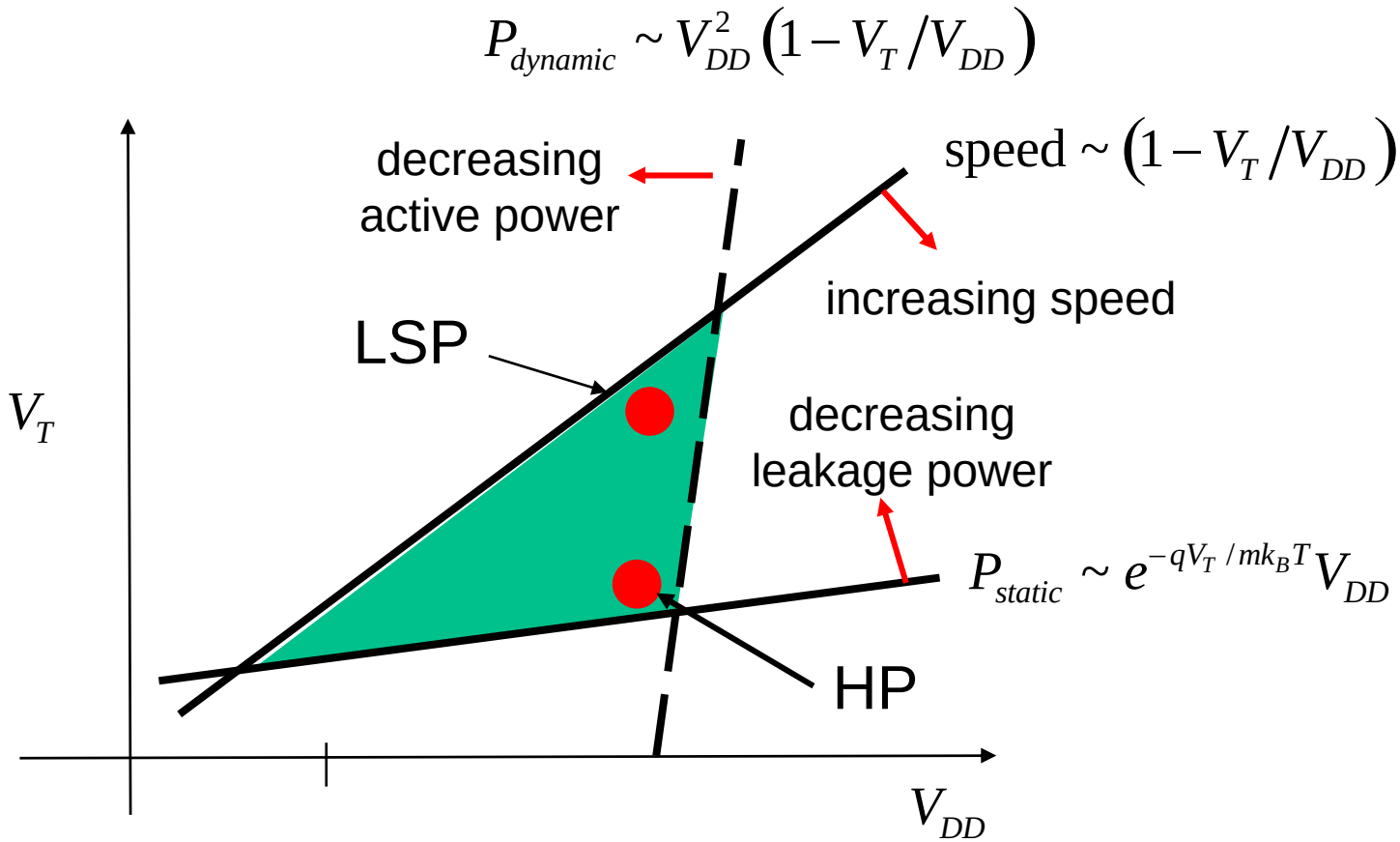
dynamic (switching) power:

$$P_{dynamic} = \alpha f C_{TOT} V_{DD}^2 \sim V_{DD}^2 (1 - V_T/V_{DD})$$

static (leakage) power:

$$P_{static} \sim I_D(\text{OFF}) V_{DD} \sim e^{-qV_T/mk_BT} V_{DD}$$

power-delay trade-off



(see Fig. 5.34 of Taur and Ning)

Outline

1) Review
2) Speed
3) Power
4) Circuit performance
5) **CMOS circuit metrics**

key metrics

1) Switching energy: $E_S = \frac{1}{2} C V_{DD}^2$

2) Switching delay: $\tau_S = \frac{C V_{DD}}{I_D(\text{ON})}$

3) Dynamic power: $P_D = \alpha f C V_{DD}^2$

4) Energy-delay product: $E_S \tau = \frac{1}{2} \frac{C^2 V_{DD}^3}{I_D(\text{on})}$

the energy-delay metric

Energy-delay product:

$$E_S\tau = \frac{1}{2}\frac{C^2V_{DD}^3}{I_D(\text{on})} \sim \frac{V_{DD}^3}{\left(V_{DD}-V_T\right)}$$

Minimum energy-delay product:

$$\frac{\partial\left(E_S\tau\right)}{\partial V_{DD}} = 0 \Rightarrow V_{DD}^{opt} = 1.5V_T$$

device metrics for 65 nm technology node

1) Switching energy: $E_S = \frac{1}{2} C V_{DD}^2 \approx 21 \text{ aJ}$

2) Switching delay: $\tau_S = \frac{C V_{DD}}{I_D(\text{ON})} = 0.64 \text{ ps}$

3) Dynamic power: $P_D = \alpha f C V_{DD}^2$

4) Energy-delay product: $E_S \tau = \frac{1}{2} \frac{C^2 V_{DD}^3}{I_D(\text{on})} = 1.4 \times 10^{-29} \text{ J-s}$

circuit performance (high-speed logic)

Typical power dissipation of a logic chip: 100 W

Dissipation of logic core: ≈ 20 W

$$P_{core} = N_{core}\frac{C_S V_{DD}^2}{2} f\alpha = 10^7 \times \frac{C_S \times 1^2}{2} \times \left(4 \times 10^9\right) \times 10^{-1}$$

$$C_S \approx 10 \text{ fF/node}$$

Average switching energy: $E_S \approx \frac{C_S V_{DD}^2}{2} = 6{,}000$ aJ

Energy-delay product: $E_S \tau \approx 1.5 \times 10^{-24}$ J-s

from device to circuit

	device	circuit	increase
delay:	0.64 ps	250 ps	~ 400 ×
switching energy:	21 aJ	6000 aJ	~300 ×
energy-delay:	$\sim 10^{-29}$ J-s	$\sim 10^{-24}$ J-s	~100,000 ×

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conclusions / questions

1) Device metrics aren't enough; the circuit is critical.

2) How close is CMOS to fundamental limits?