EE-612:
Lecture 24:
CMOS Circuits: Part 1

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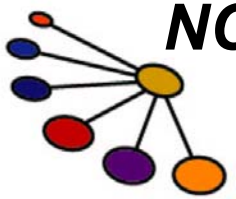

NCN

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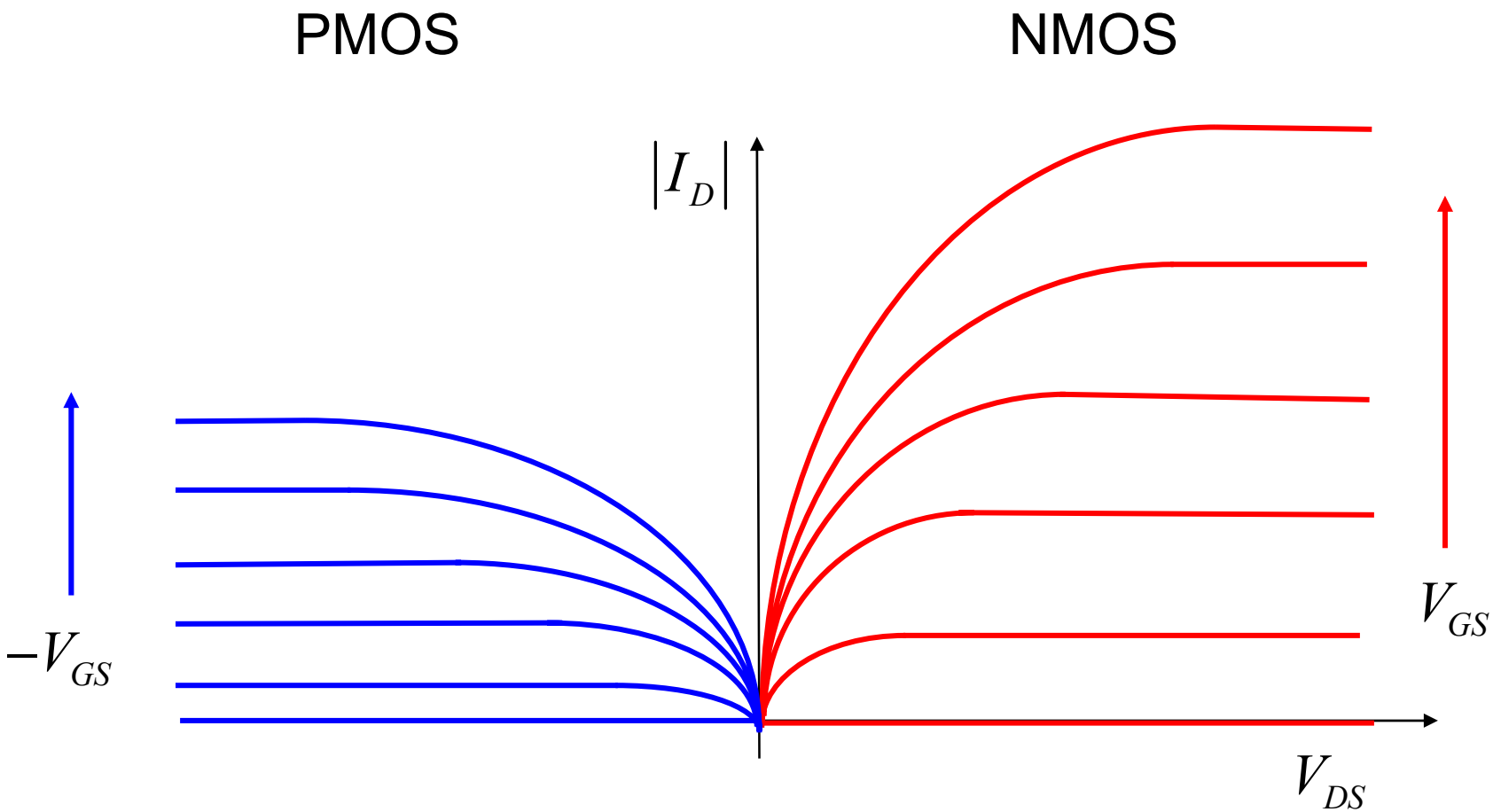
Outline

1) Review
2) CMOS circuits
3) The CMOS inverter
4) Speed

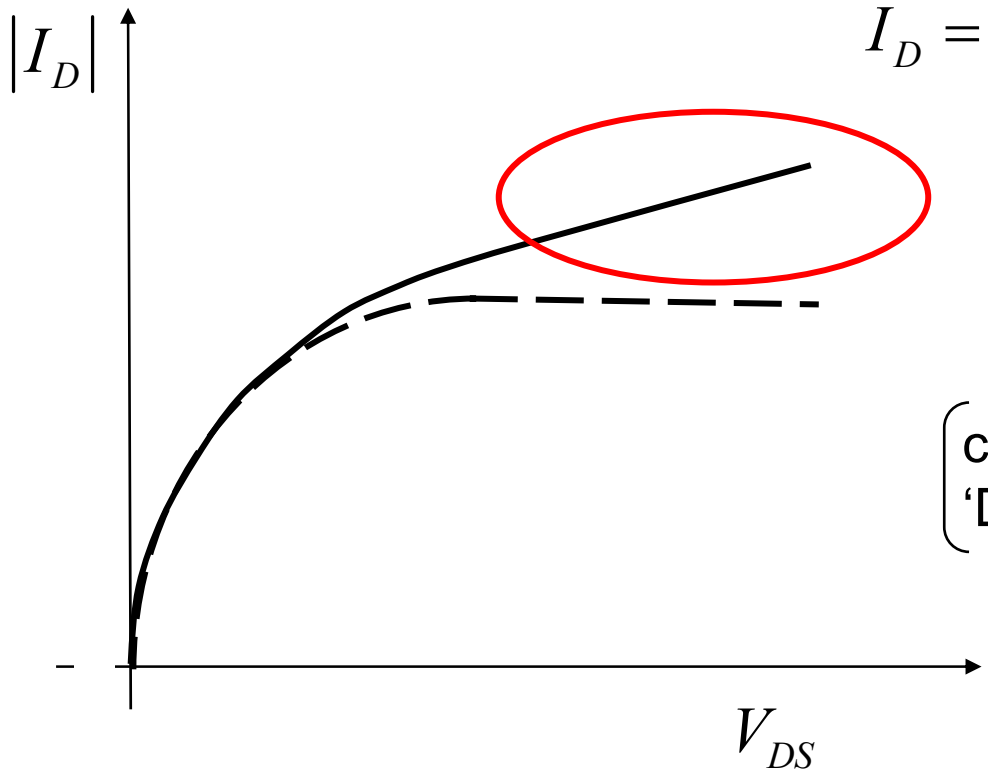
MOSFETs



output conductance

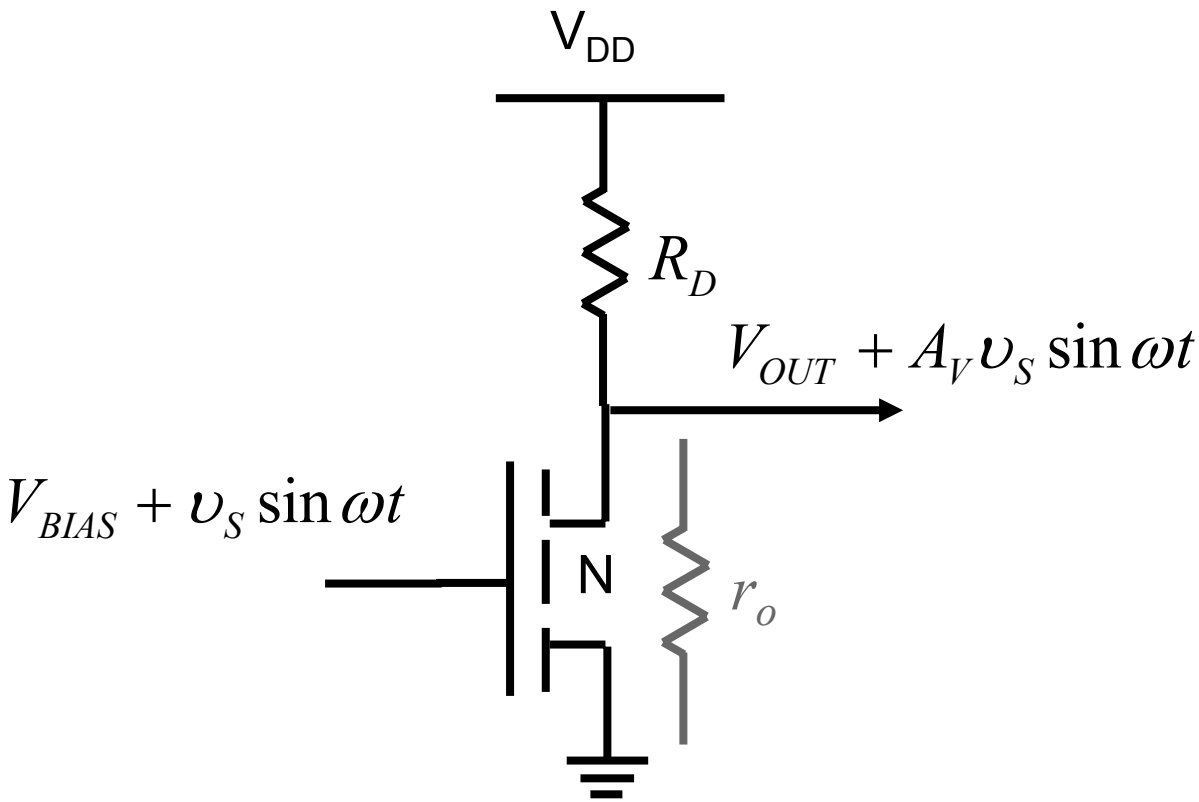
$$r_o = \left(\partial I_D / \partial V_{DS}\right)^{-1}$$

$$I_D = I_{DSAT}\left(1 + \lambda V_{DS}\right)$$



channel length modulation
'DIBL above threshold'

small signal gain



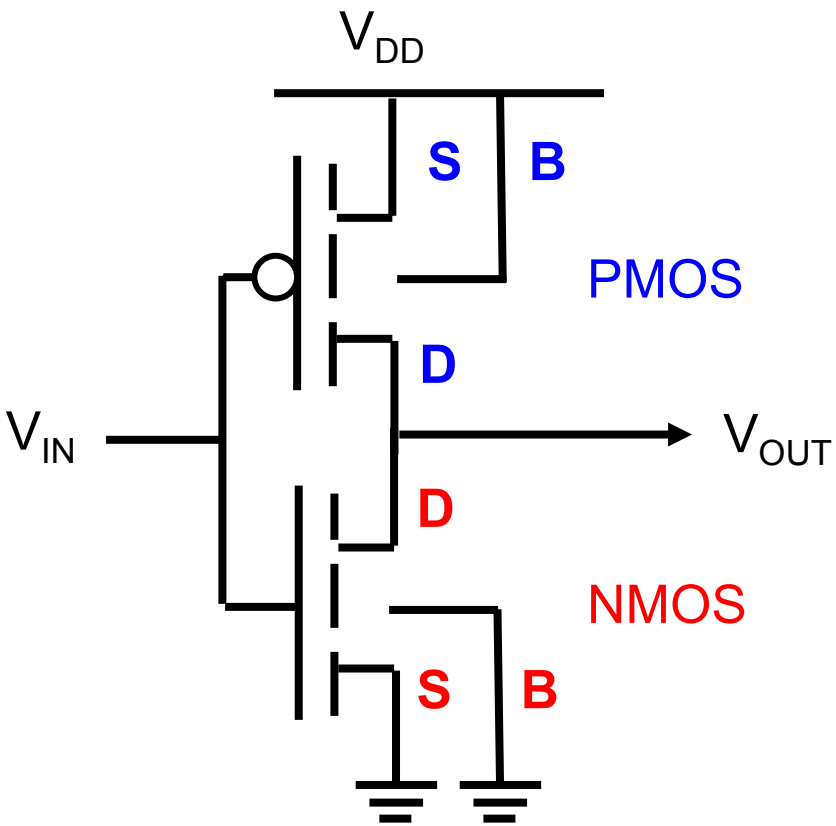
$$A_V = -g_m \left(R_D \parallel r_o \right)$$

$$g_m = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{V_{DS}}$$

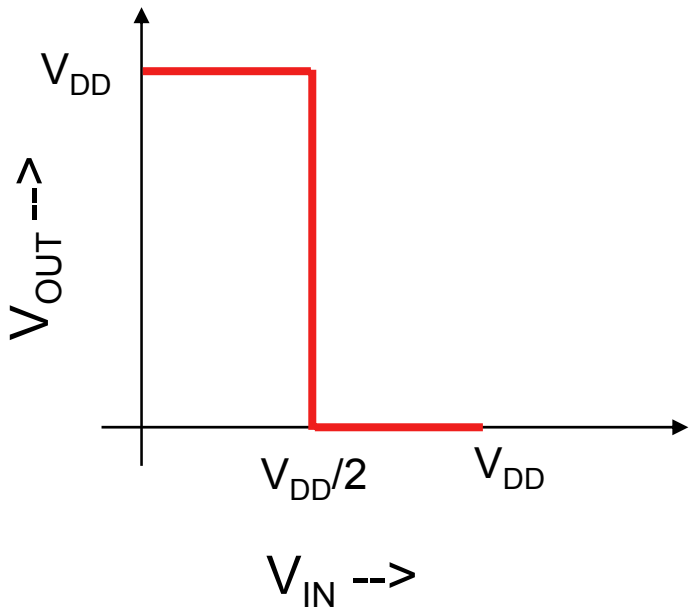
Outline

1) Review
2) **CMOS circuits**
3) The CMOS inverter
4) Speed
5) Power
6) Circuit performance

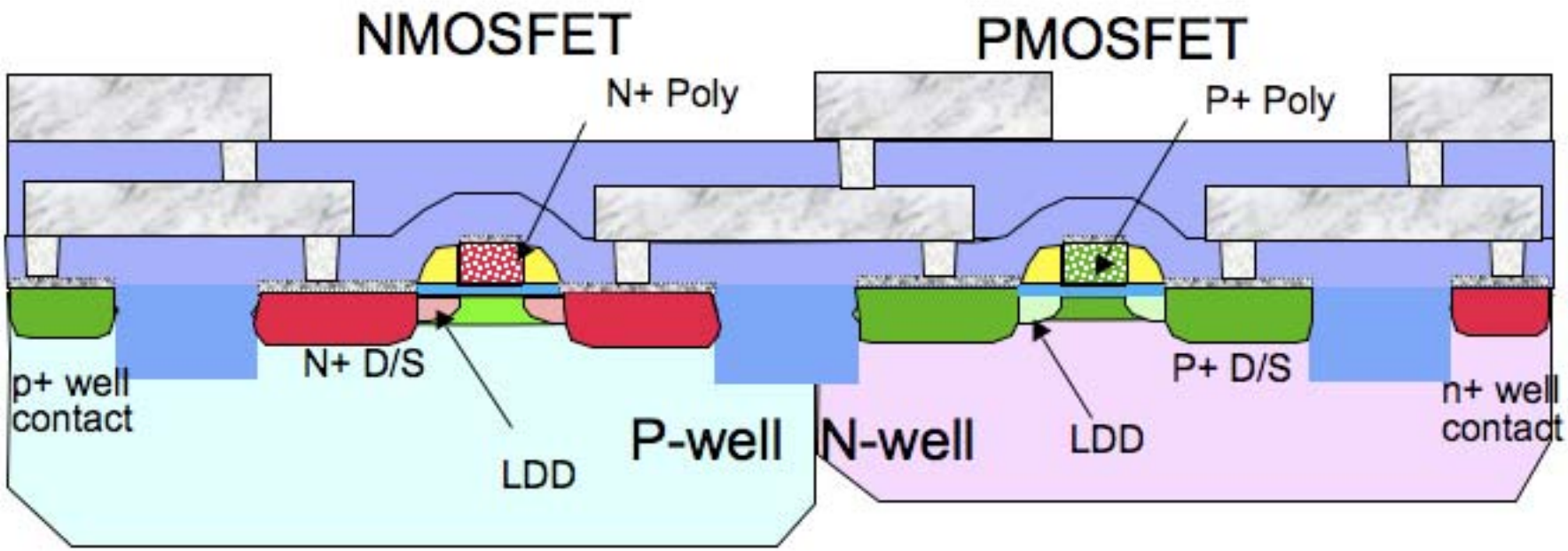
ideal CMOS inverter



transfer characteristic



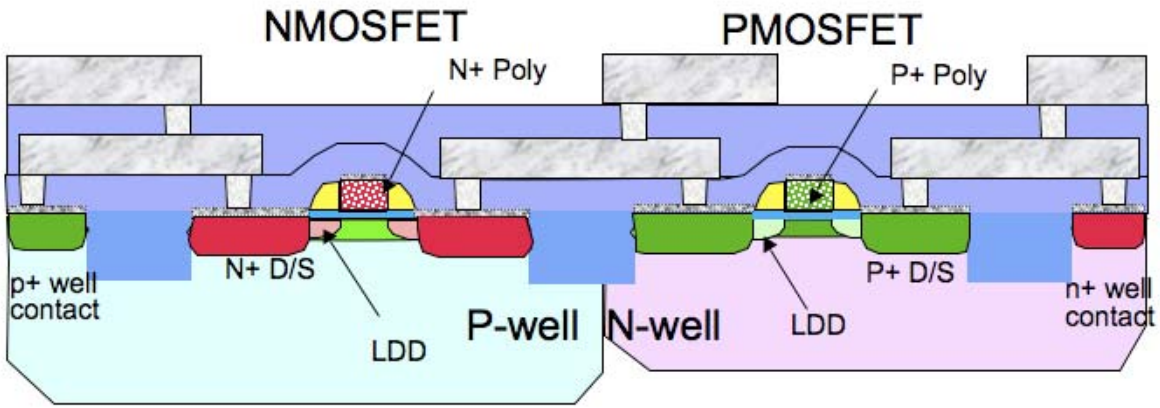
CMOS inverter (cross-section)

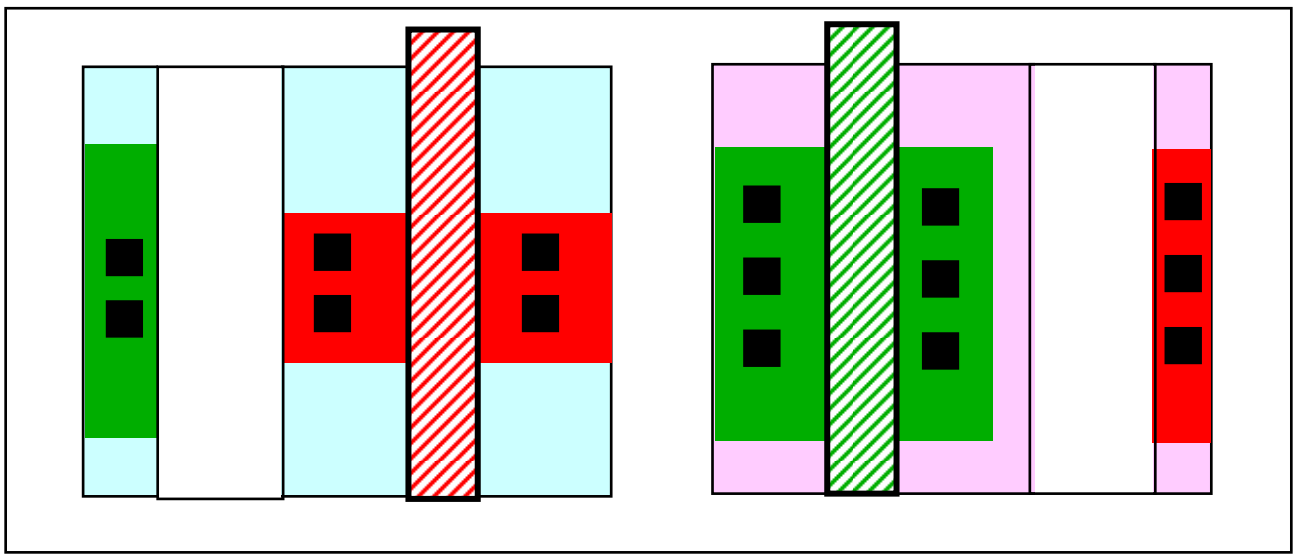


Courtesy of Dr. Lynn Fuller of Rochester Institute of Technology.

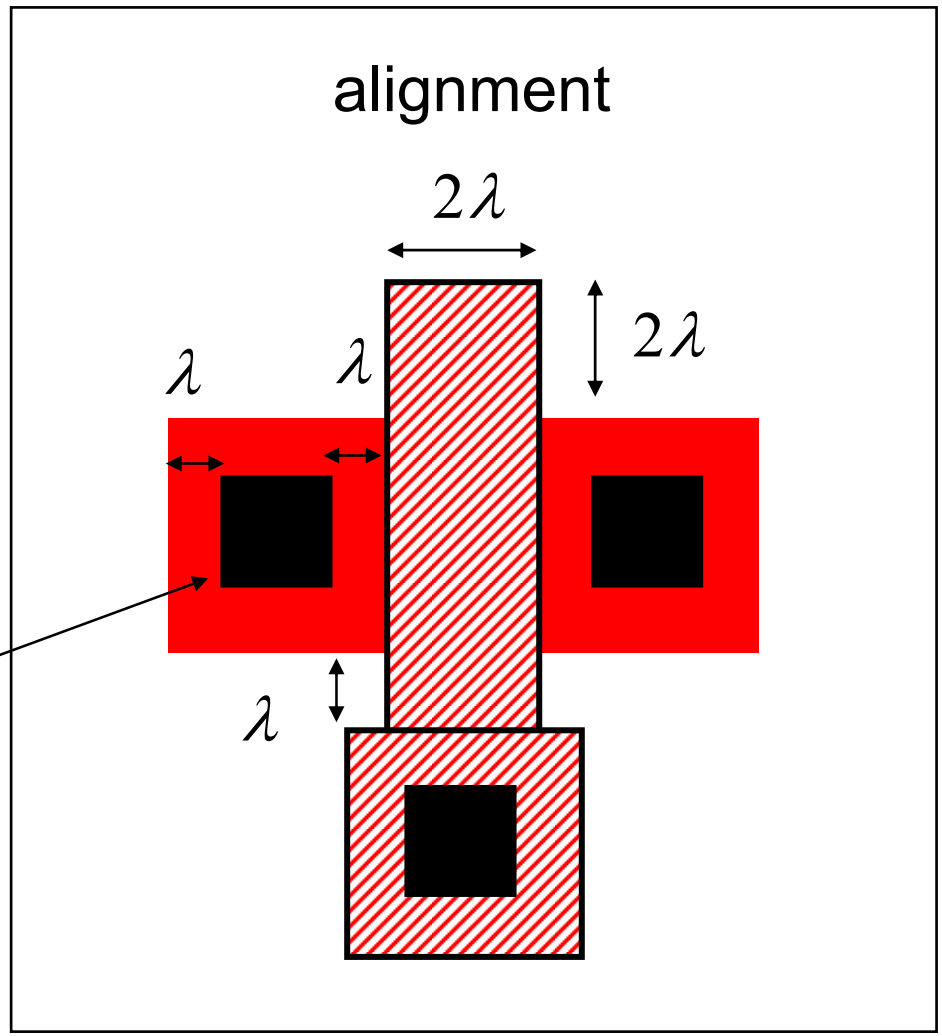
http://www.rit.edu/~lffeee/AdvCmos2003.pdf

CMOS inverter (top view)





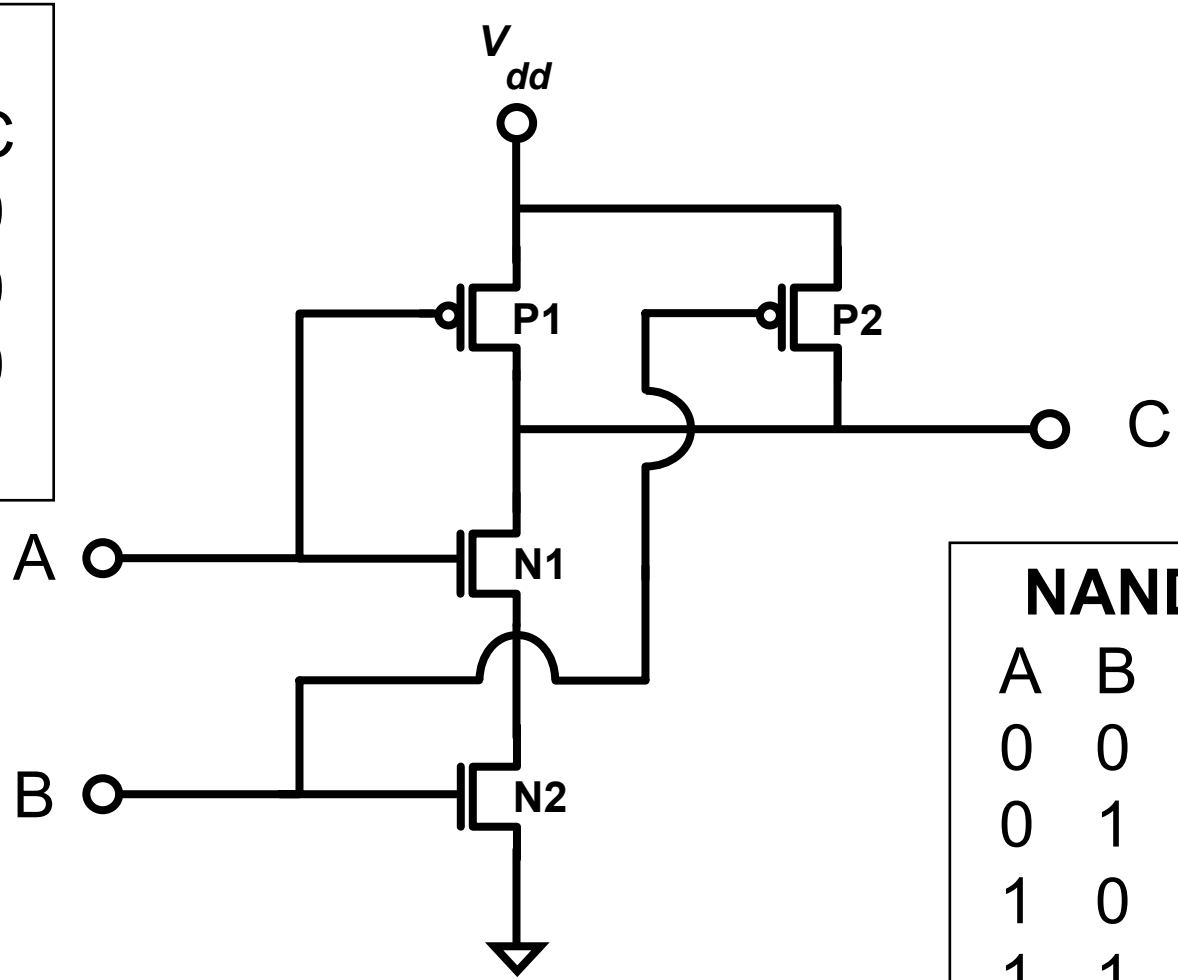
technology-independent design rules



2-input NAND gate

AND

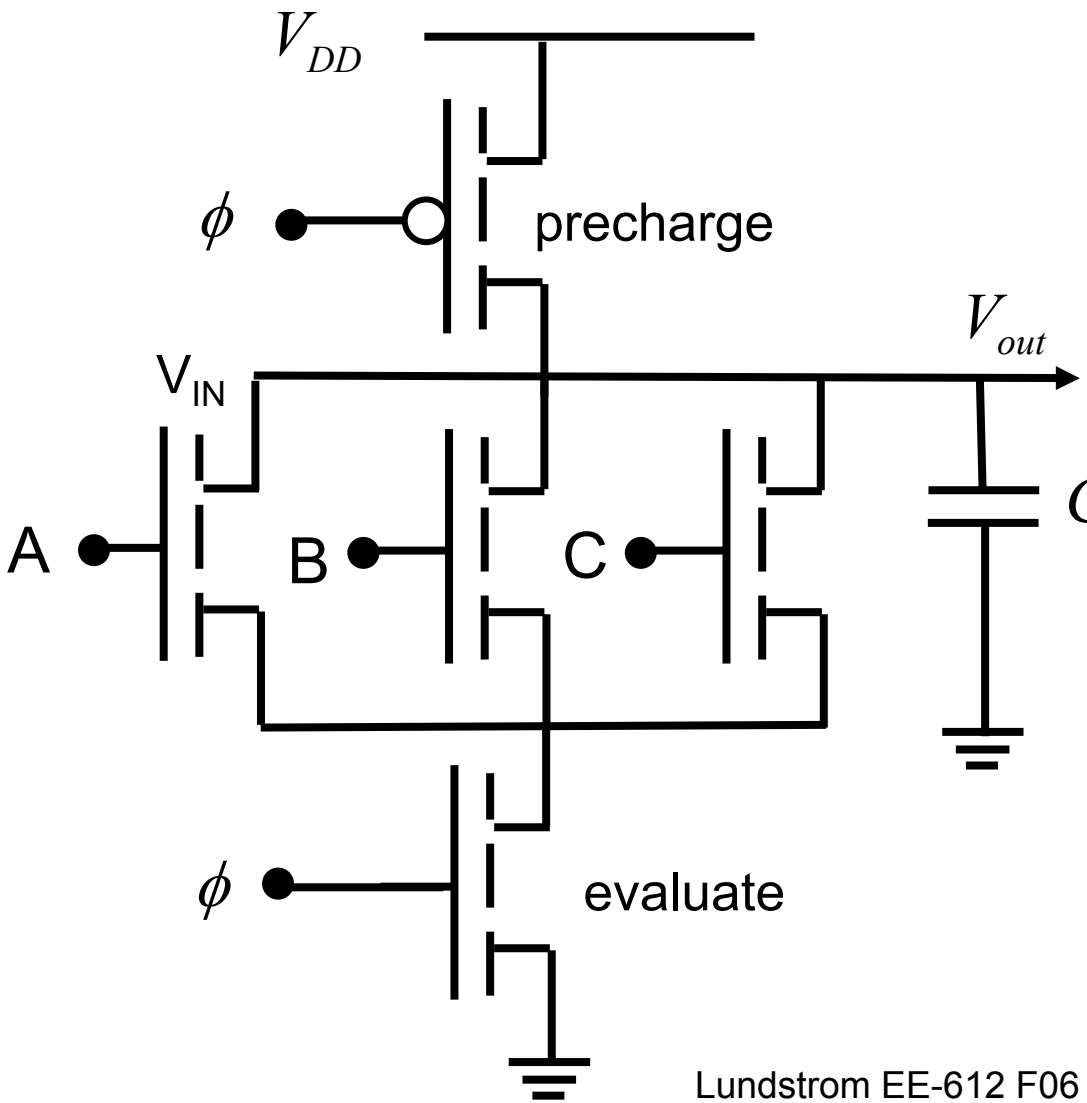
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1



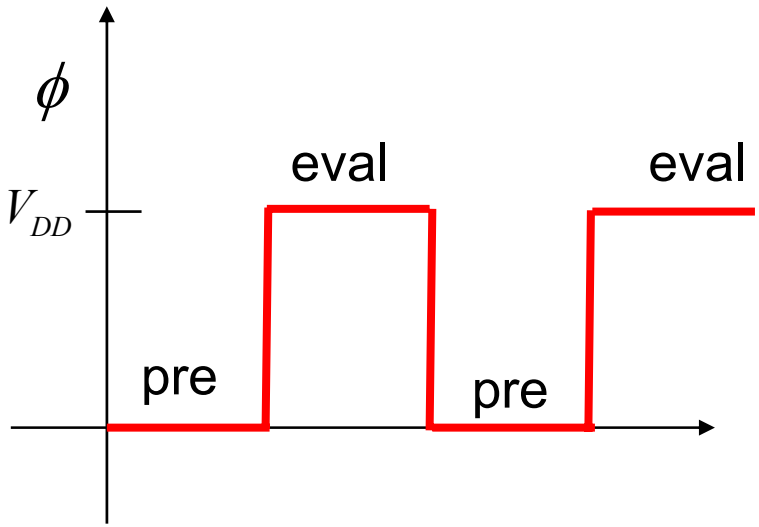
NAND

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

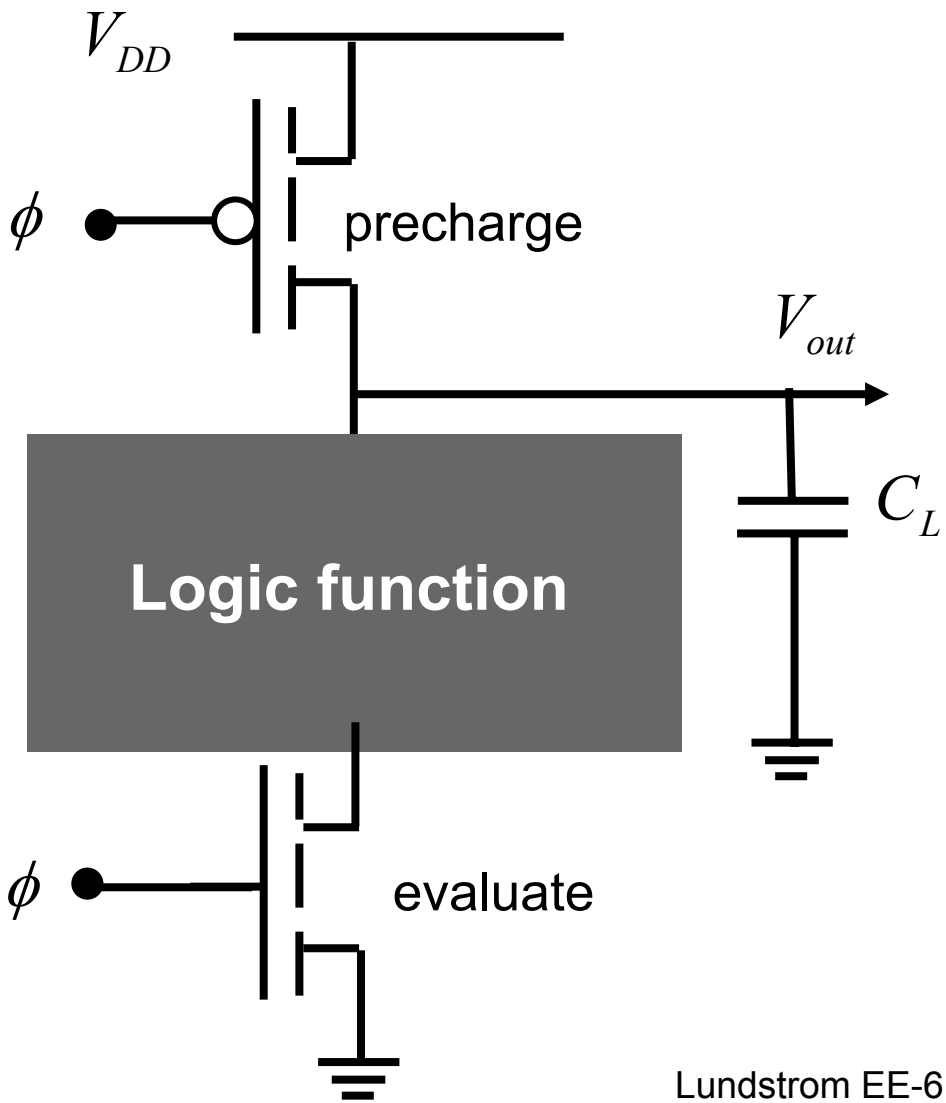
dynamic logic: NOR gate



A	B	C	OUT
0	0	0	1
0	1	0	0

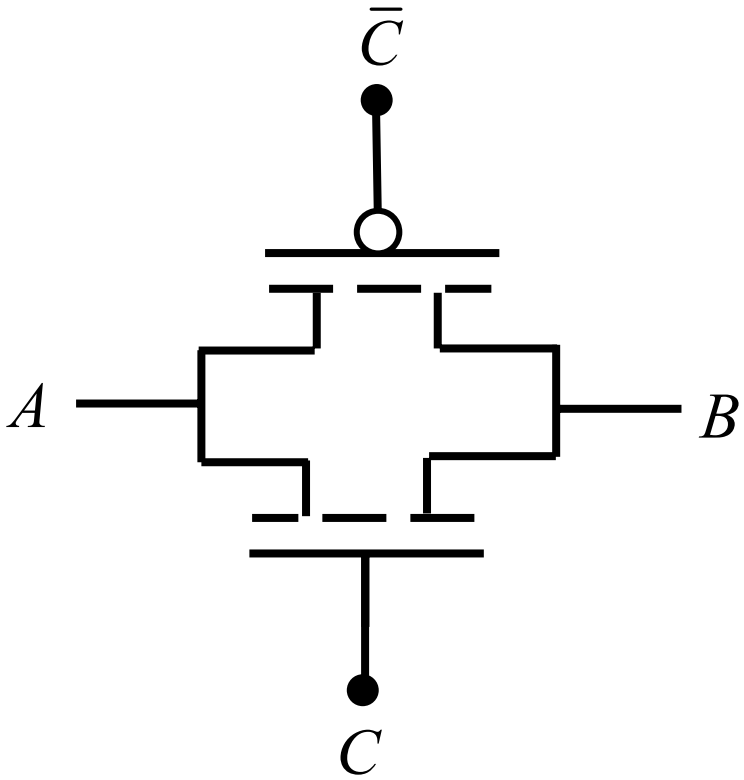


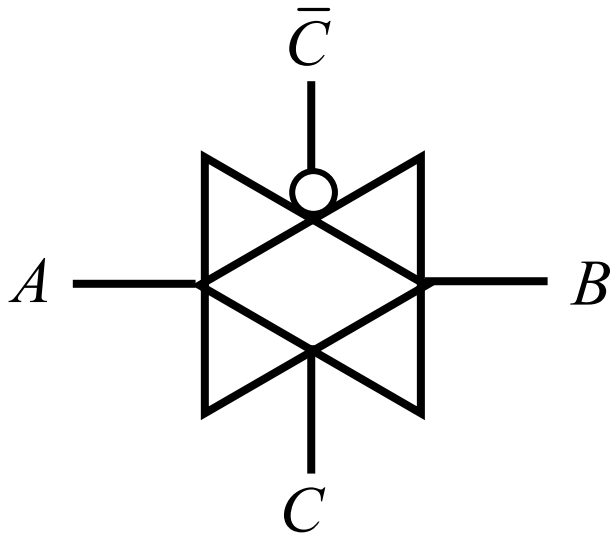
dynamic logic



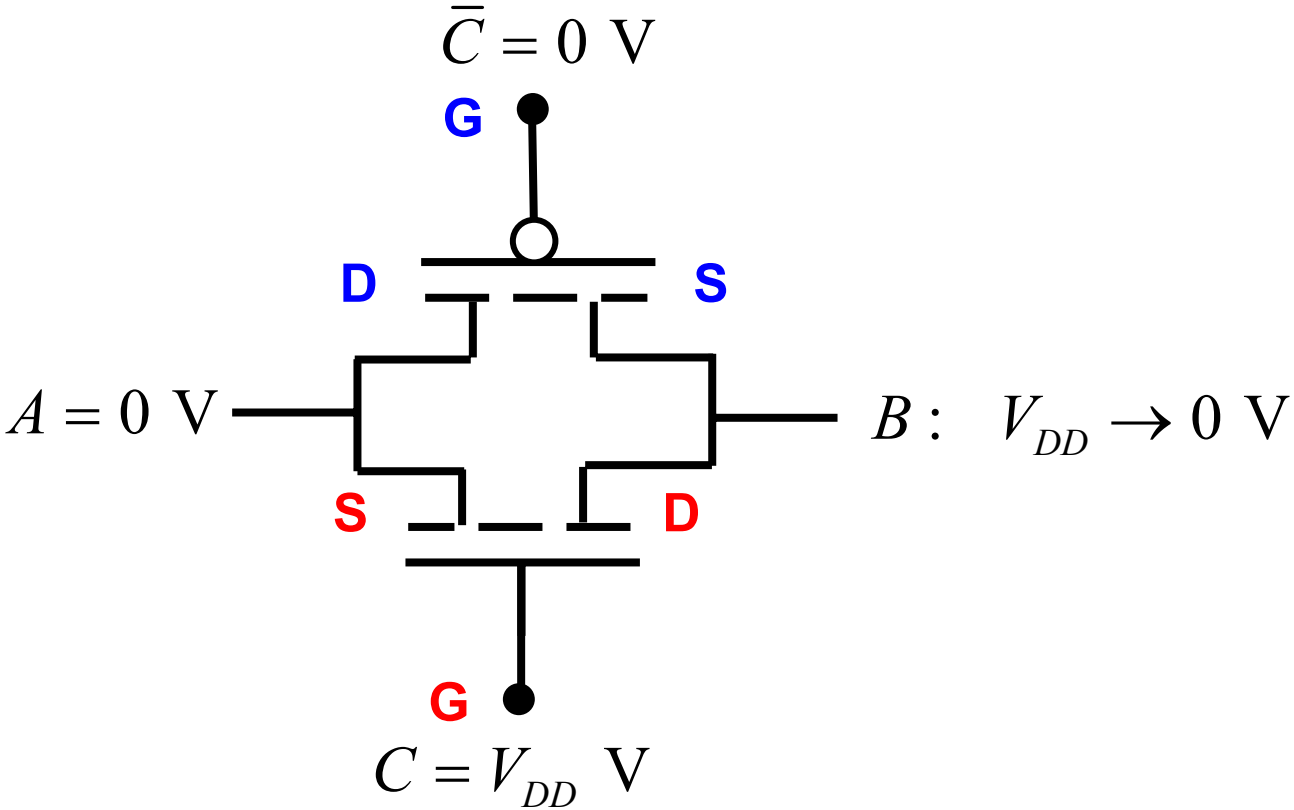
- M-input logic needs M+2 transistors (2M for CMOS)
- 'no' standby power
- minimum frequency

transmission gates



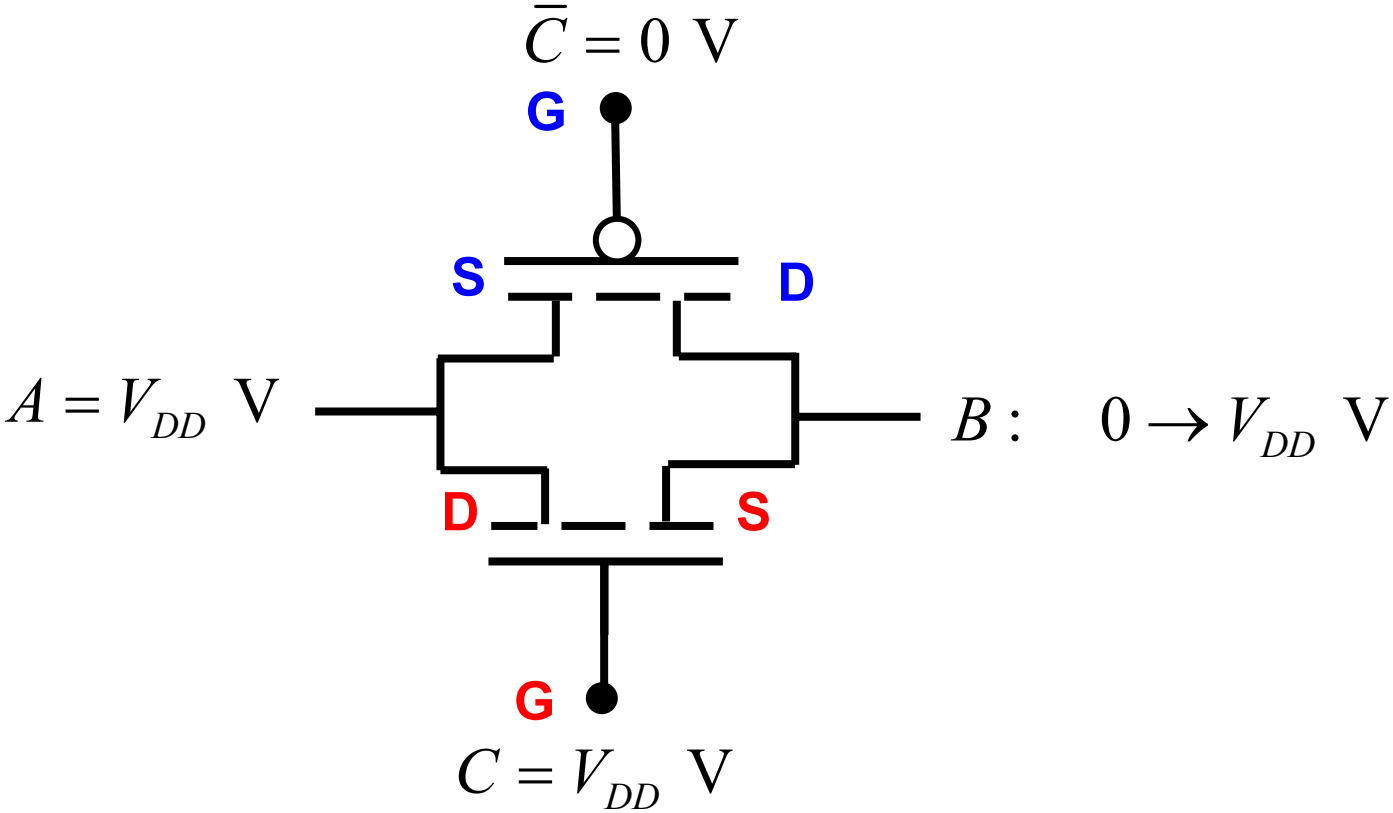


transmission gates: high to low



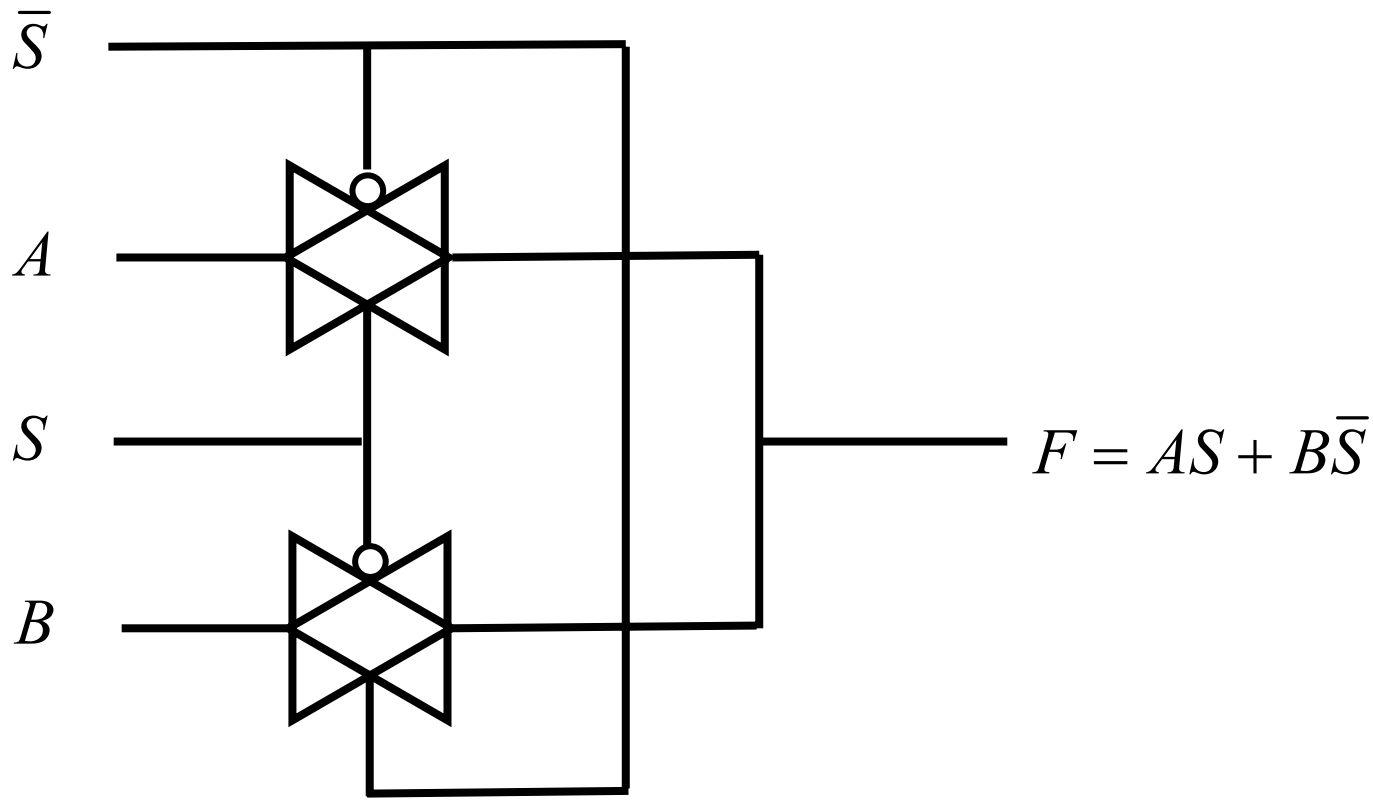
NMOS can discharge the output all the way to 0V; PMOS can't.

transmission gates: low to high



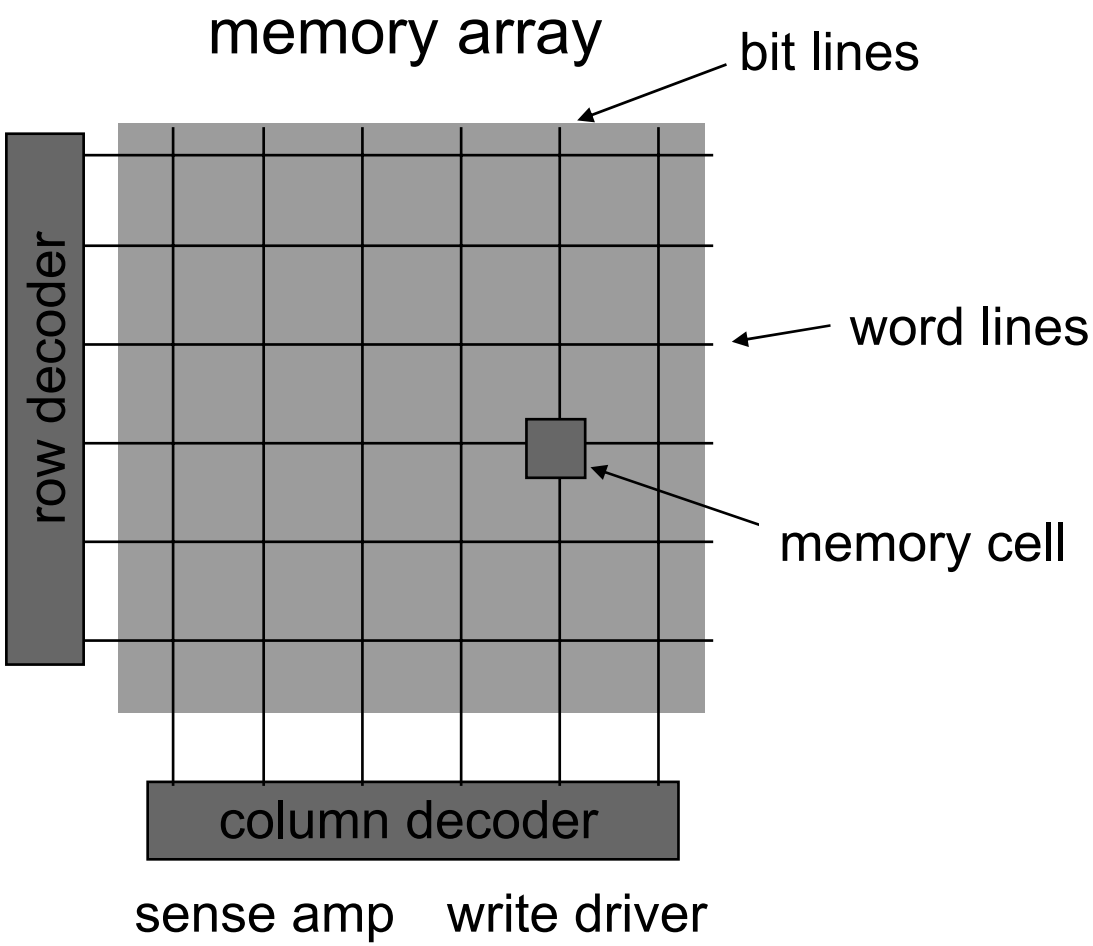
PMOS can charge the output all the way to V_{DD} V; NMOS can't.

multiplexer with transmission gates



From Hodges, Jackson, and Saleh, *Analysis and Design of Digital Integrated Circuits, 3rd Ed.,* McGraw-Hill, 2004.

memories

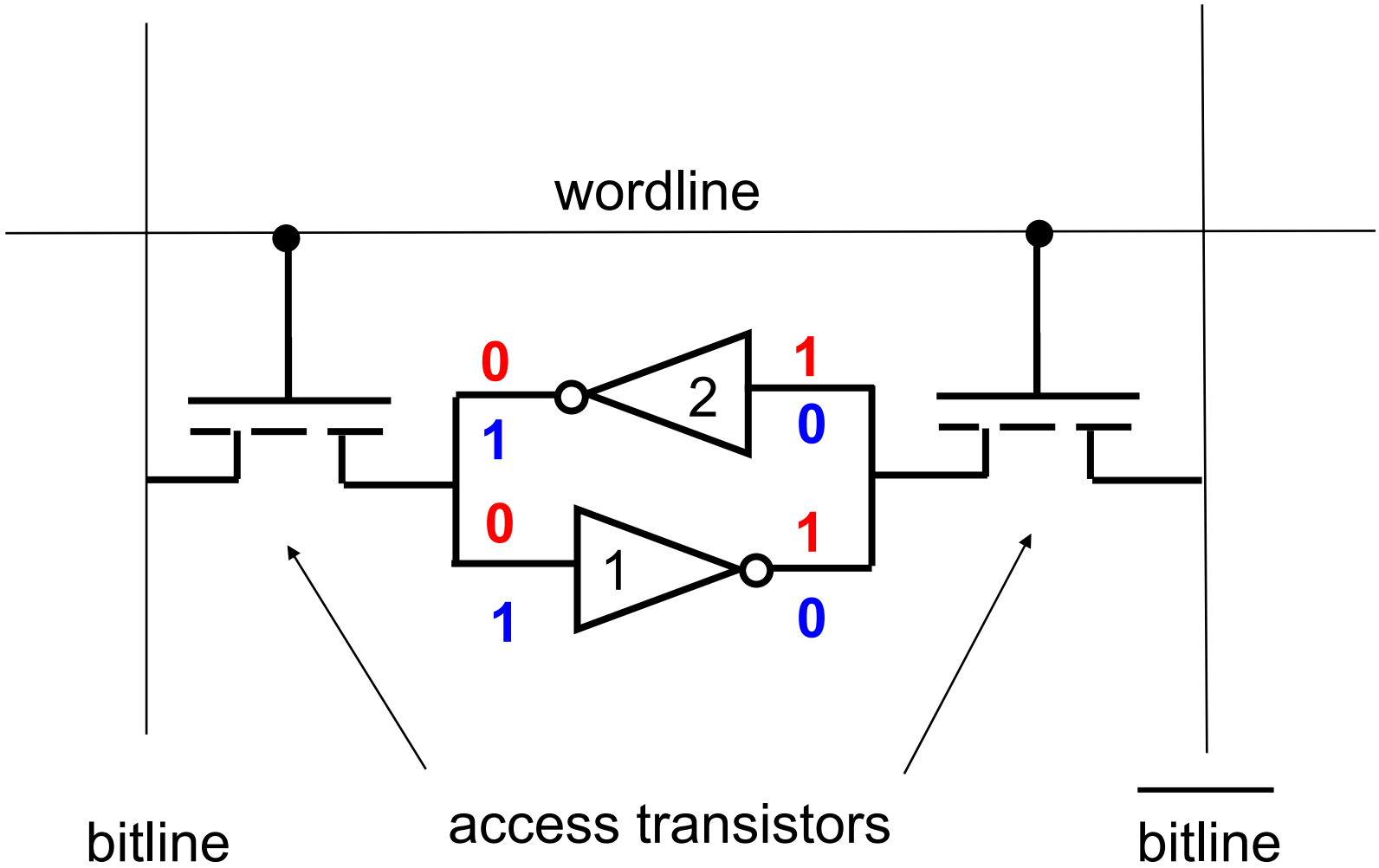


SRAM

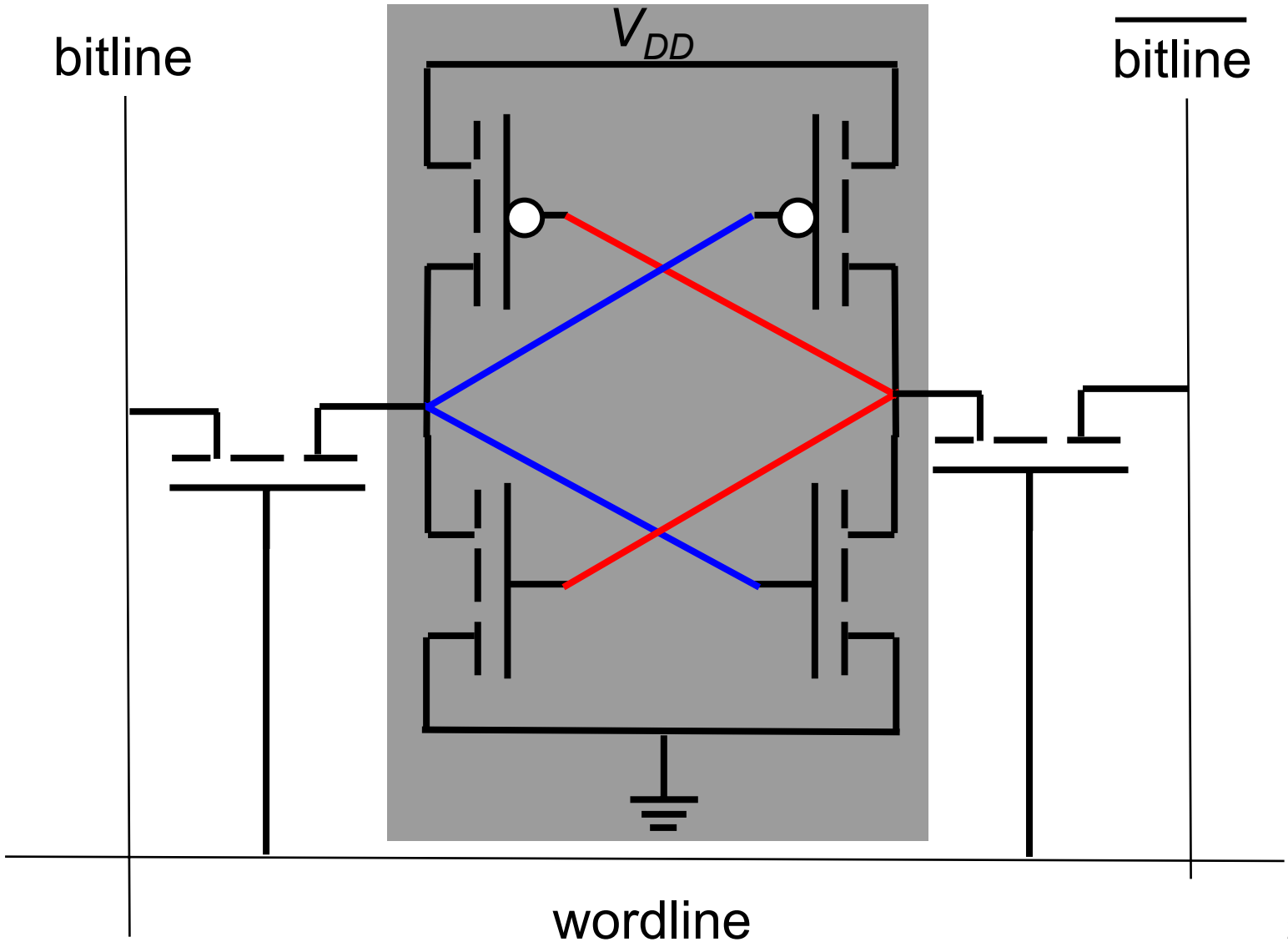
DRAM

Flash, etc.

SRAM cell



6 transistor SRAM cell



6 transistor SRAM cell (ii)

- SRAM consumes most of the area on a CPU chip
- steady state power determined by leakage (use high V_T)
- small area with optimized layout
- minimum W/L - sensitive to variations

for more information on CMOS circuits

Hodges, Jackson, and Saleh,
Analysis and Design of Digital Integrated Circuits, 3rd Ed.,
McGraw-Hill, 2004.

Outline

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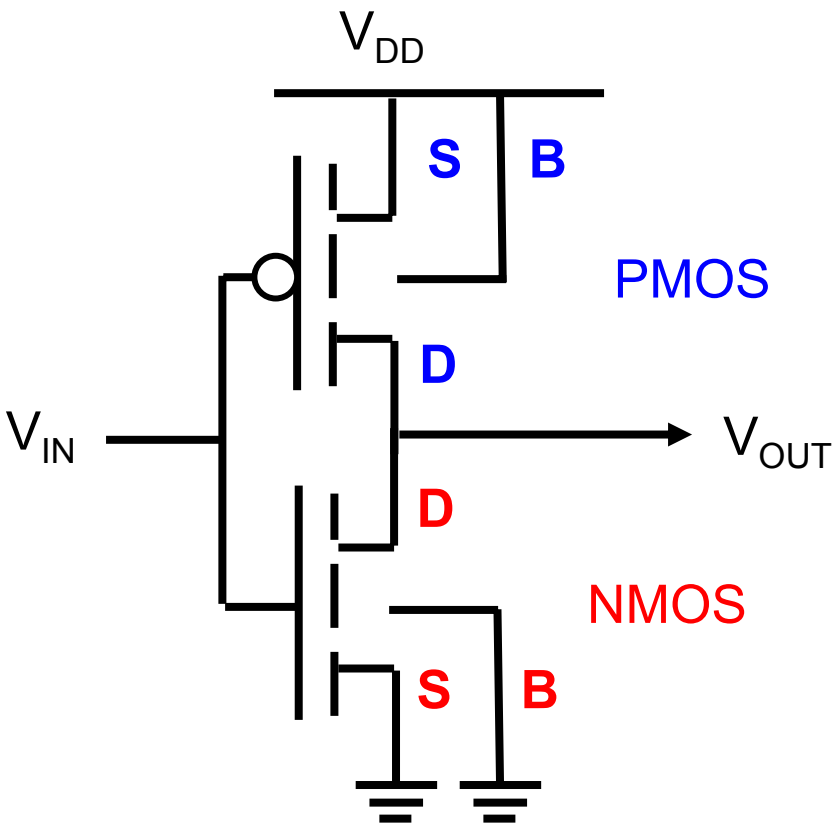
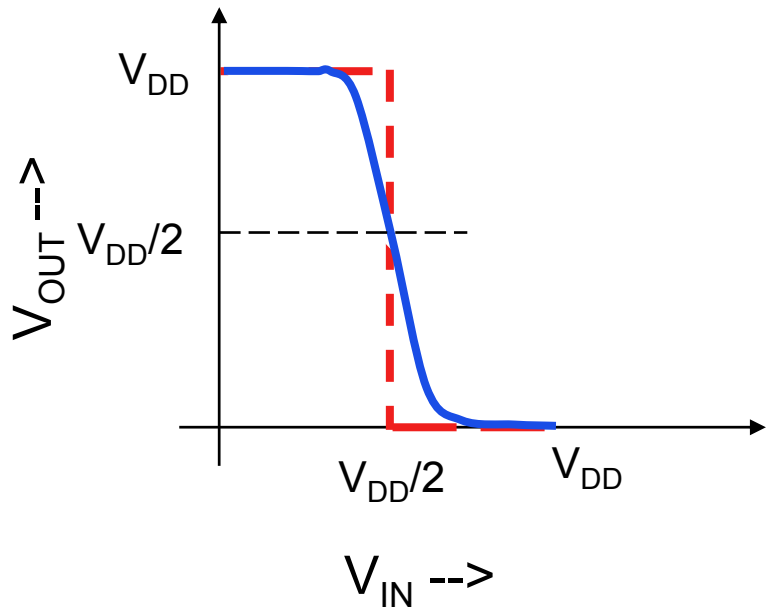
2) CMOS circuits
3) **The CMOS inverter**
4) Speed

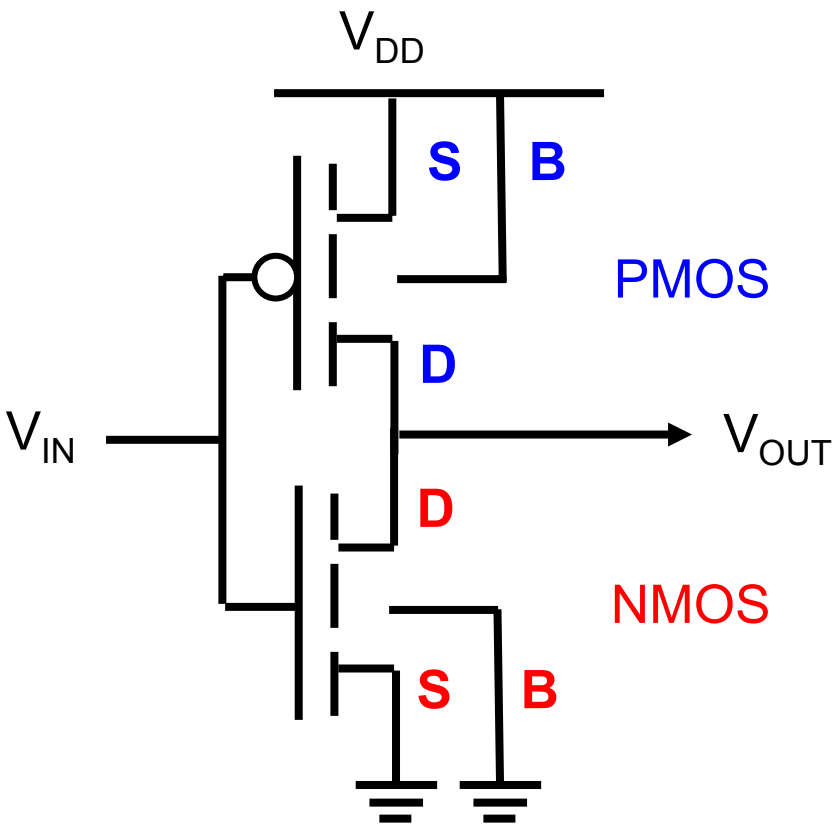
CMOS inverter



transfer characteristic



CMOS inverter: voltages



$$V_{gs} = V_{in} - V_{DD}$$

$$V_{ds} = V_{out} - V_{DD}$$

$$V_{gs} = V_{in}$$

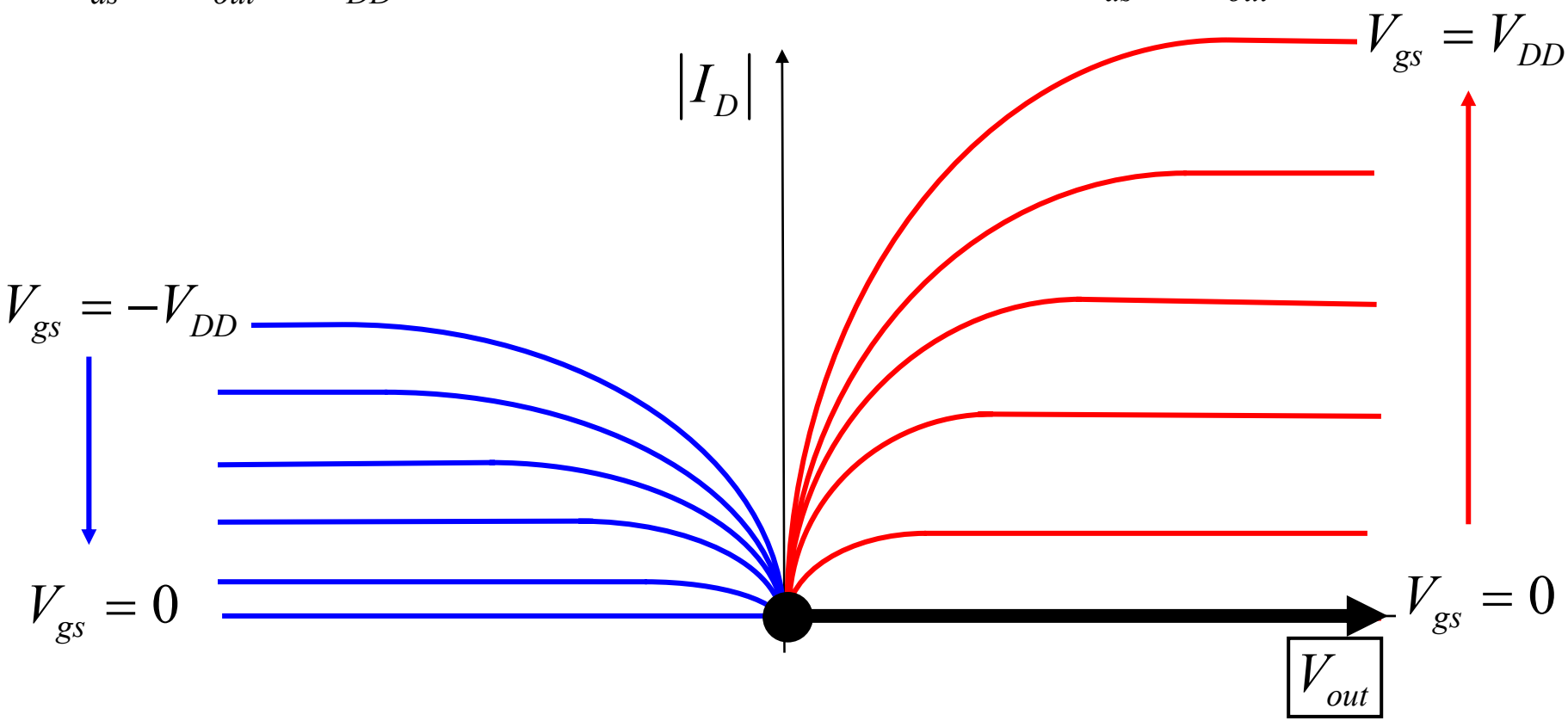
$$V_{ds} = V_{out}$$

CMOS inverter: transfer characteristic

$$V_{gs} = V_{in} - V_{DD}$$
$$V_{ds} = V_{out} - V_{DD}$$

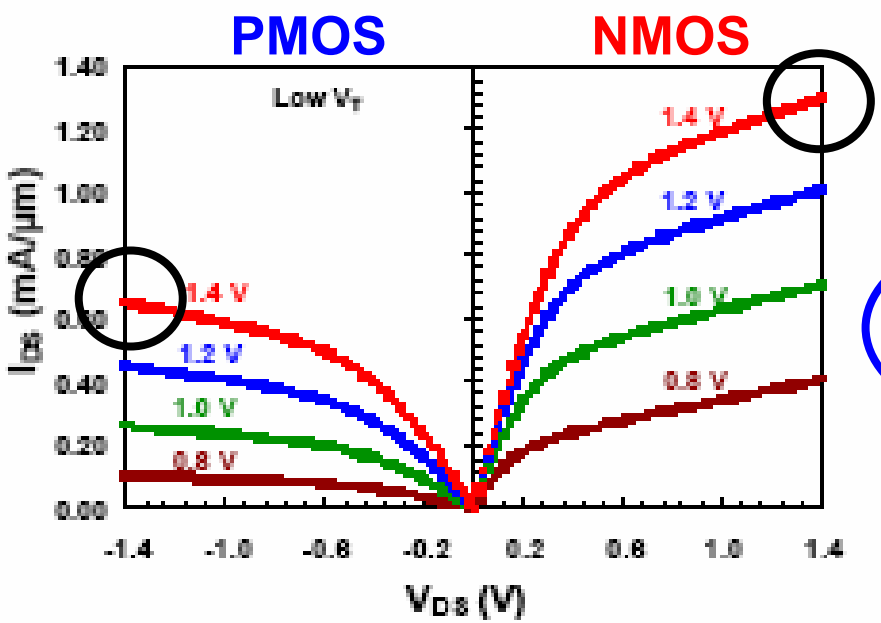
$$V_{in}: \quad 0 \rightarrow V_{DD}$$

$$V_{gs} = V_{in}$$
$$V_{ds} = V_{out}$$



sizing the P-MOSFET

130 nm technology (L_G = 60 nm)



$$W_P \approx 2W_N$$

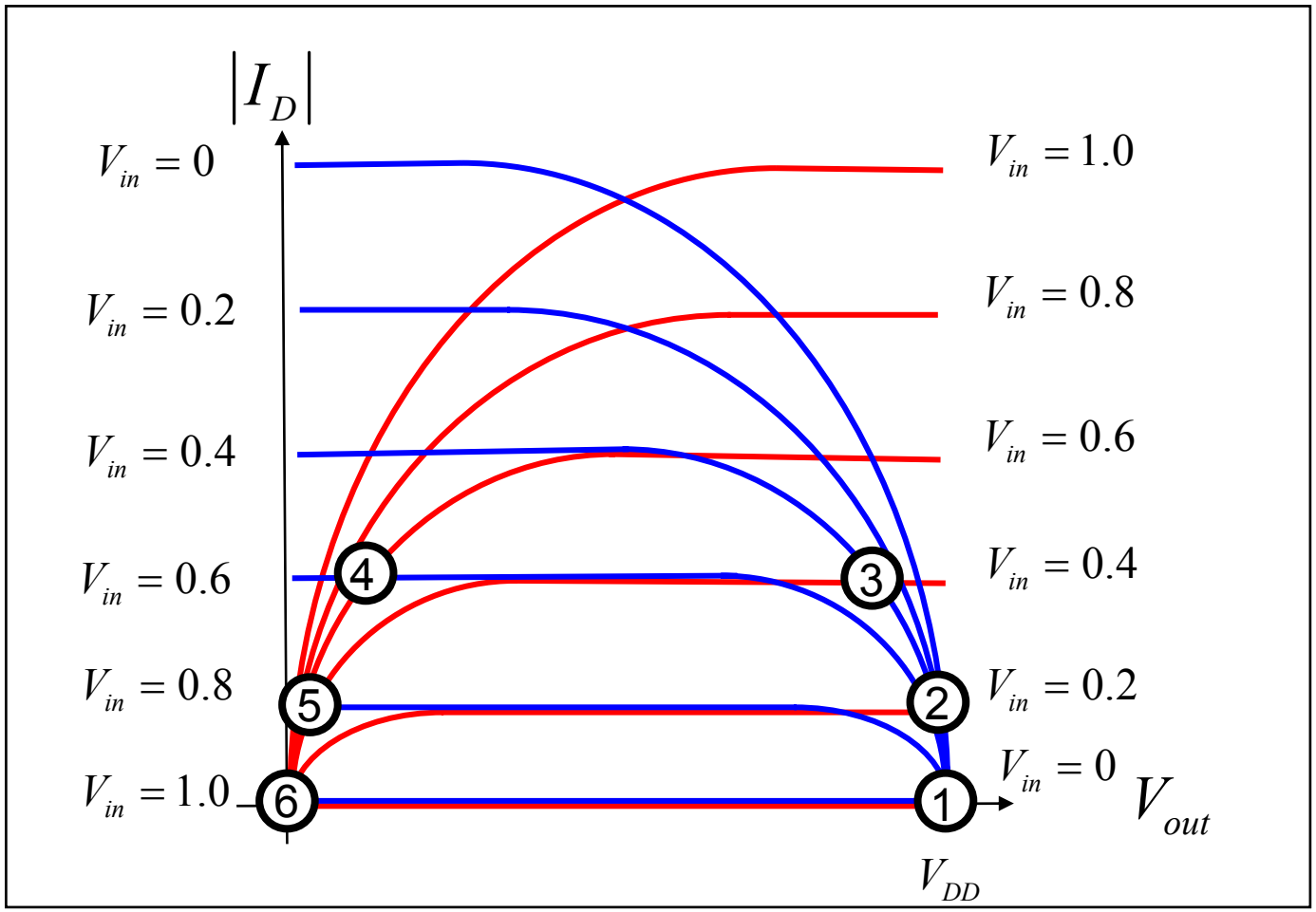
I-V curves for low V_T device

Intel Technical J., Vol. 6, May 16, 2002.

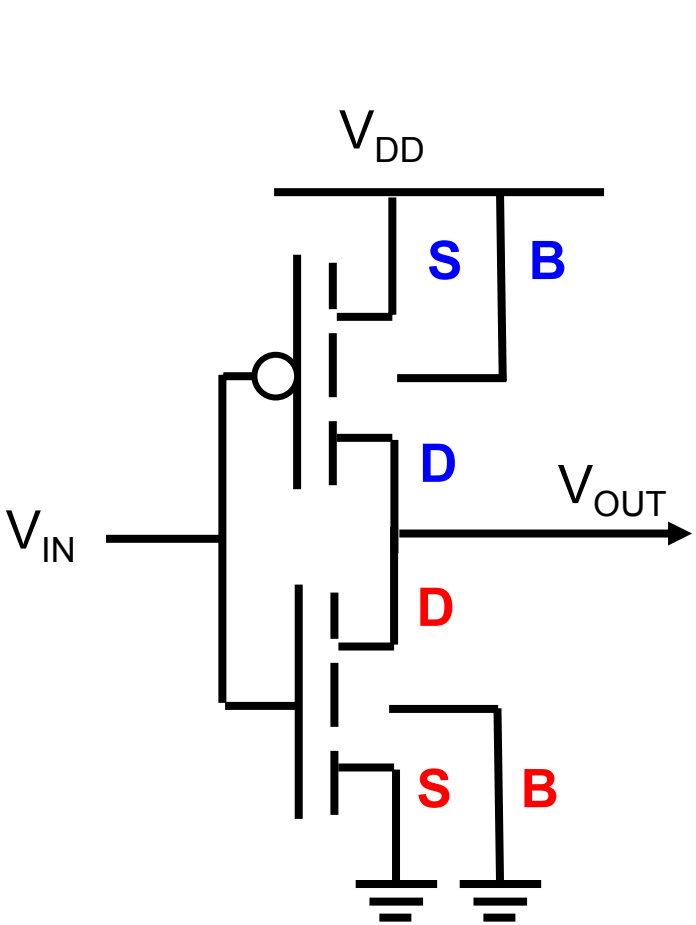
CMOS inverter: V_{out} vs. V_{in}

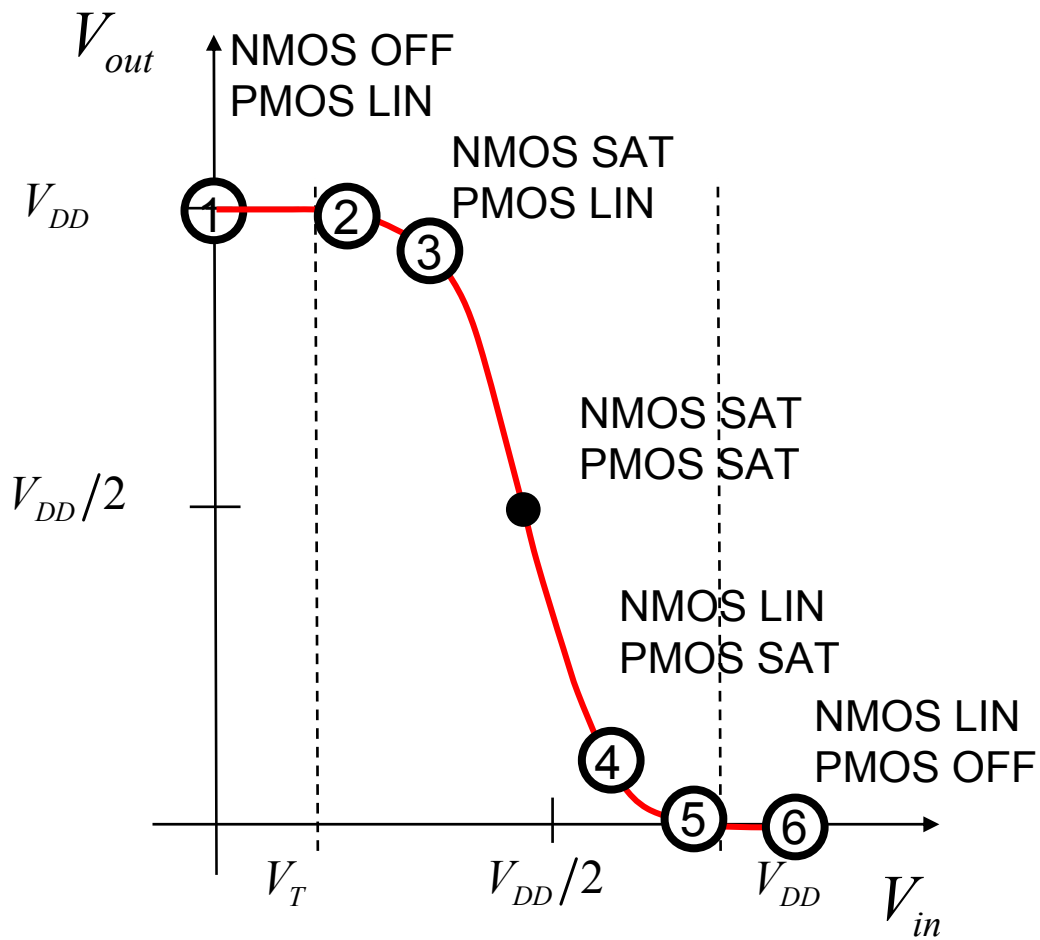
$V_{DD} = 1.0$ V

$V_{TN} = -V_{TP} = 0.15$ V

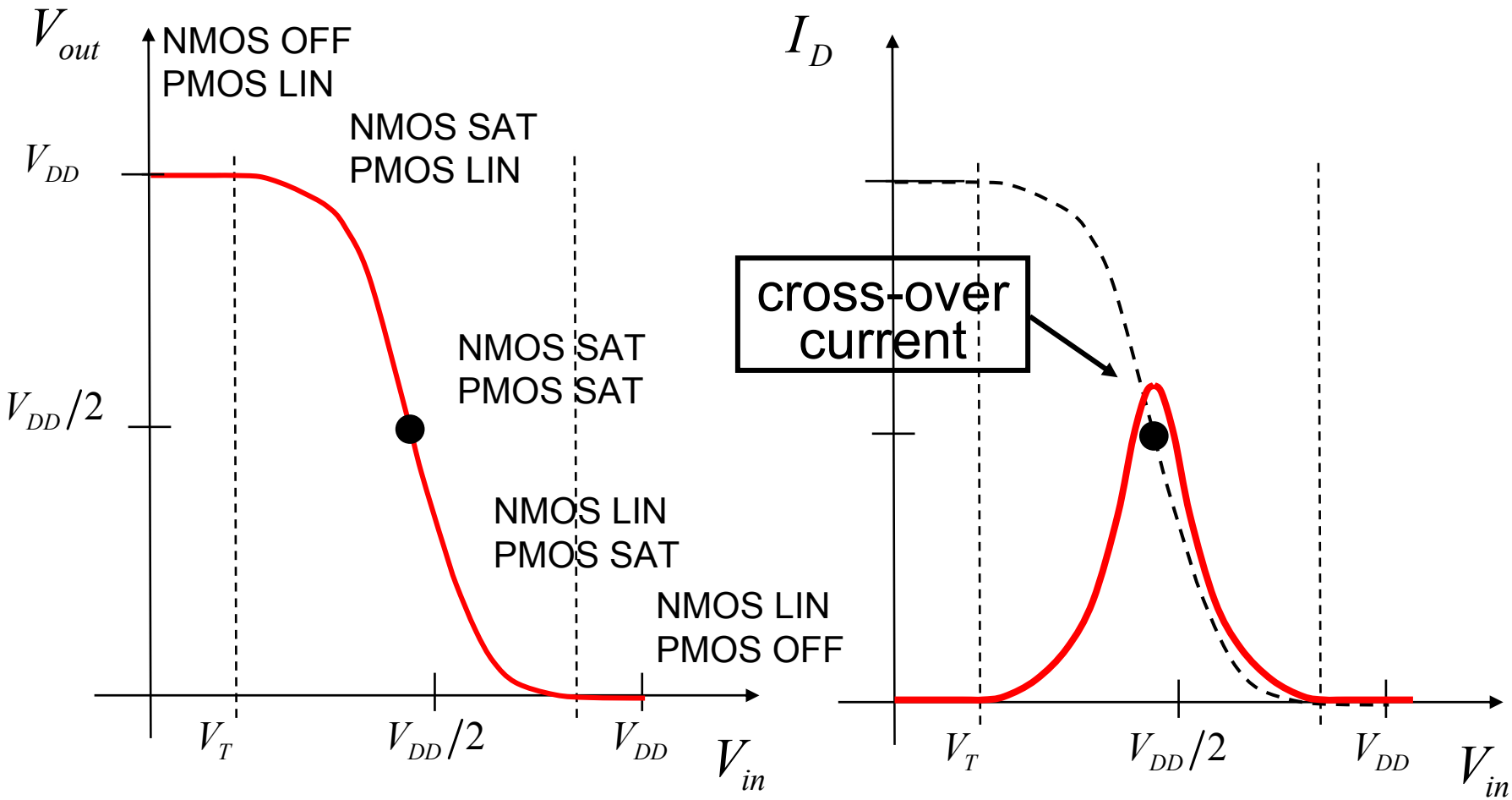


CMOS VTC

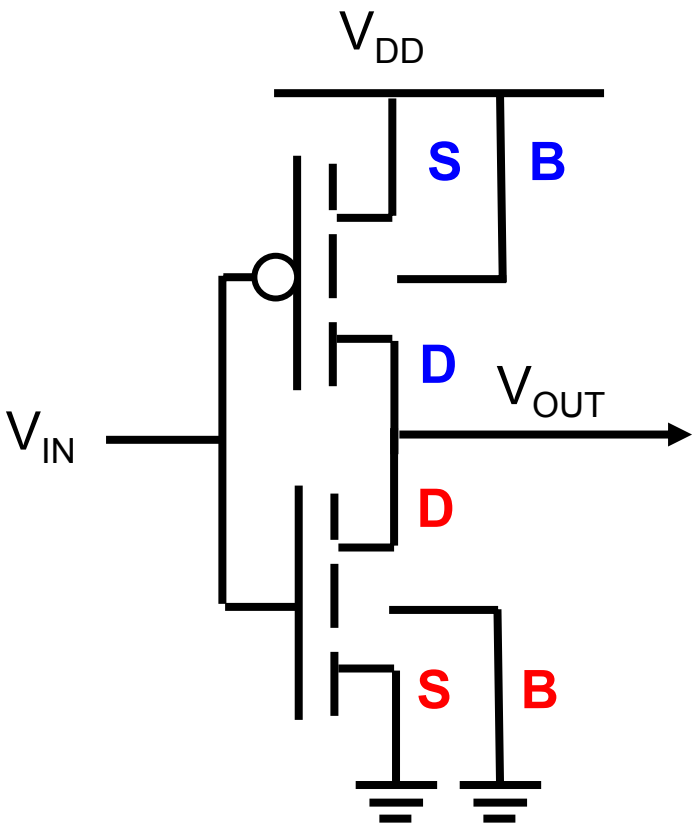

V_DD
S
B
D
V_OUT
V_IN
D
S
B

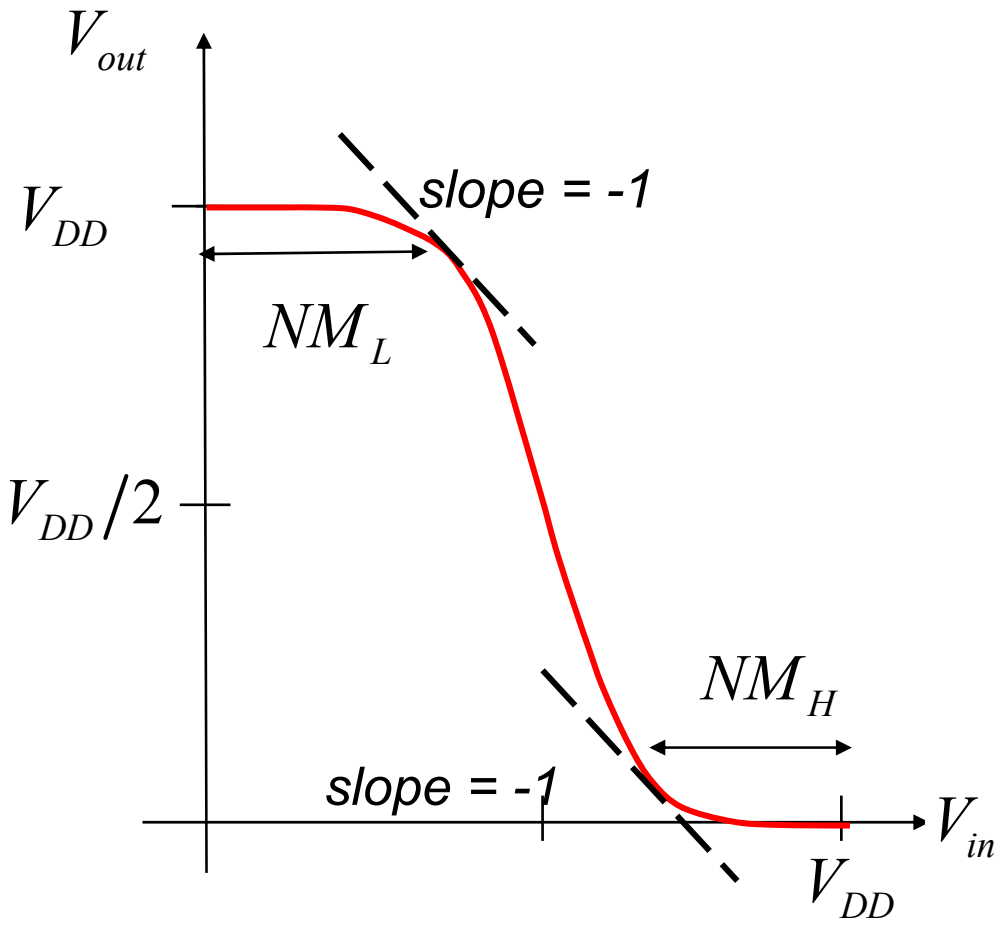

V_out
NMOS OFF
PMOS LIN
NMOS SAT
PMOS LIN
V_DD
1
2
3
NMOS SAT
PMOS SAT
V_DD/2
NMOS LIN
PMOS SAT
NMOS LIN
PMOS OFF
4
5
6
V_T
V_DD/2
V_DD
V_in

CMOS inverter: current

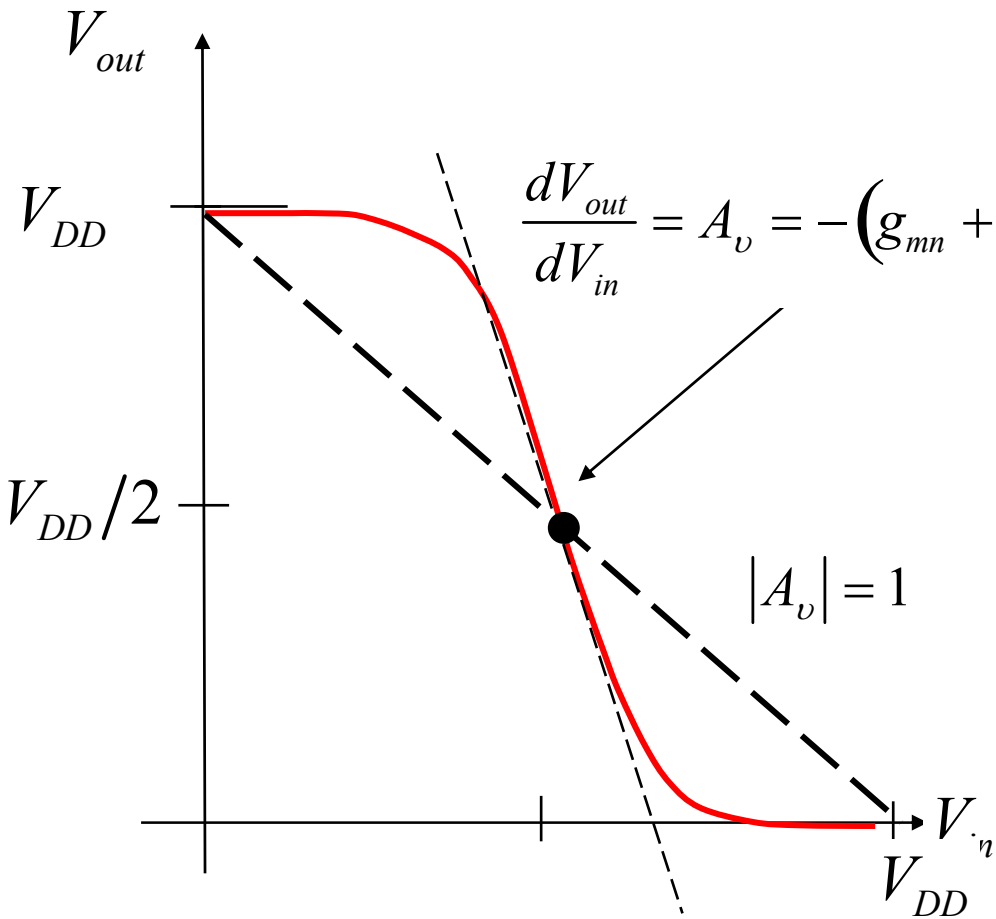


CMOS inverter: noise margins



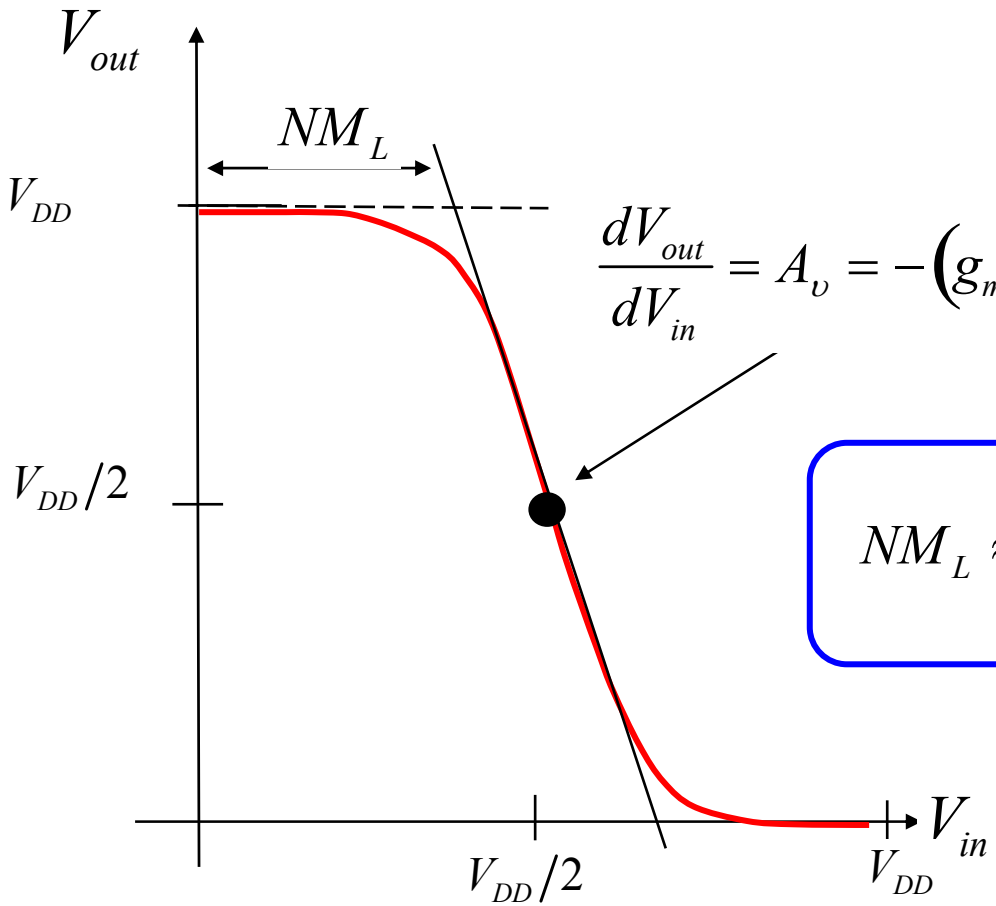


importance of gain



must have gain to have noise margins

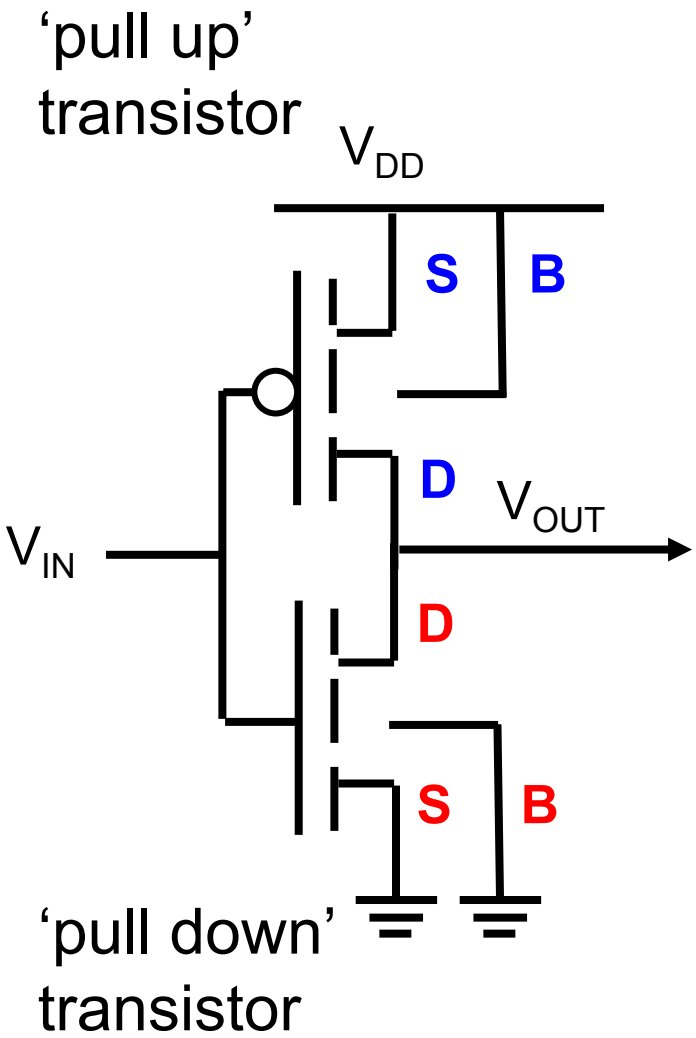
approximate noise margins



$$\frac{dV_{out}}{dV_{in}} = A_\upsilon = -\left(g_{mn} + g_{mp}\right)\left(r_{on} \parallel r_{op}\right)$$

$$NM_L \approx NM_H \approx \frac{V_{DD}}{2}\left(1 - \frac{1}{|A_\upsilon|}\right)$$

CMOS inverter: summary



1) little current flow (power dissipation) unless switching

2) good noise margins if device has high R_{OUT} (high gain)

next: understand speed and power

Outline

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2) CMOS circuits
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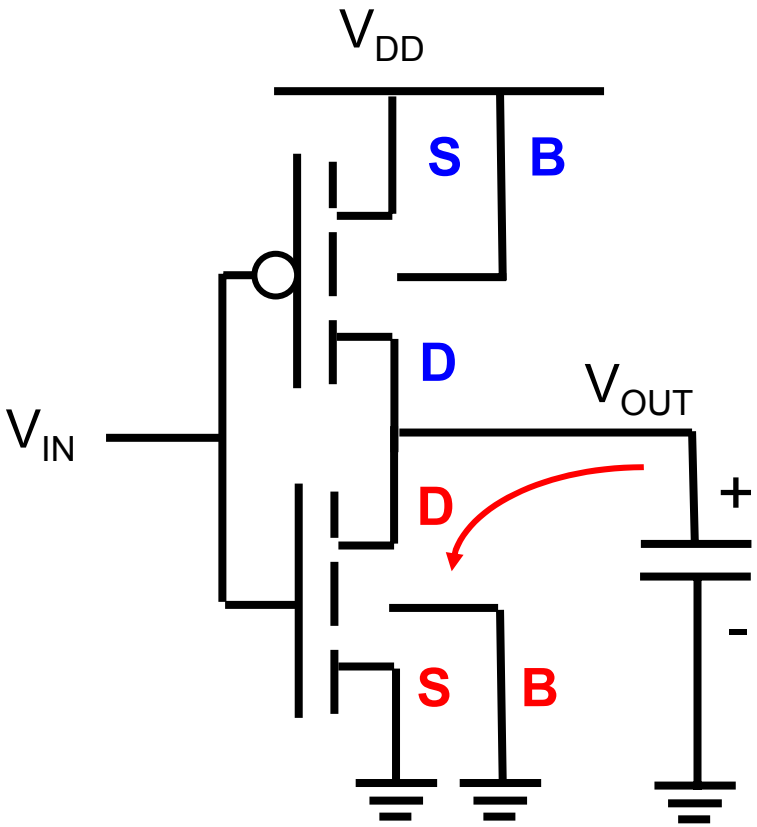
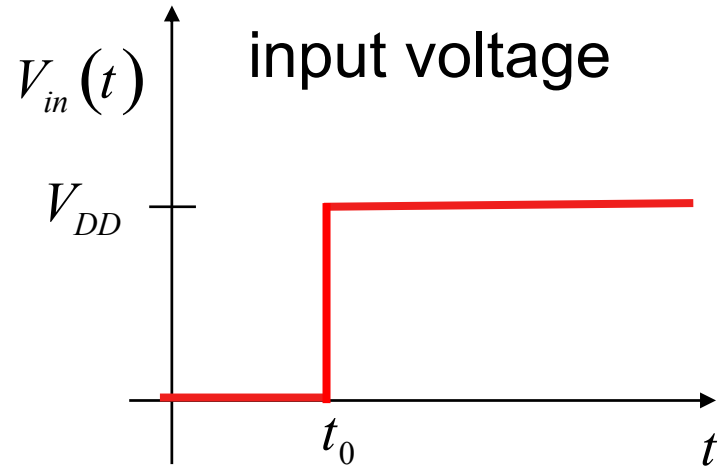
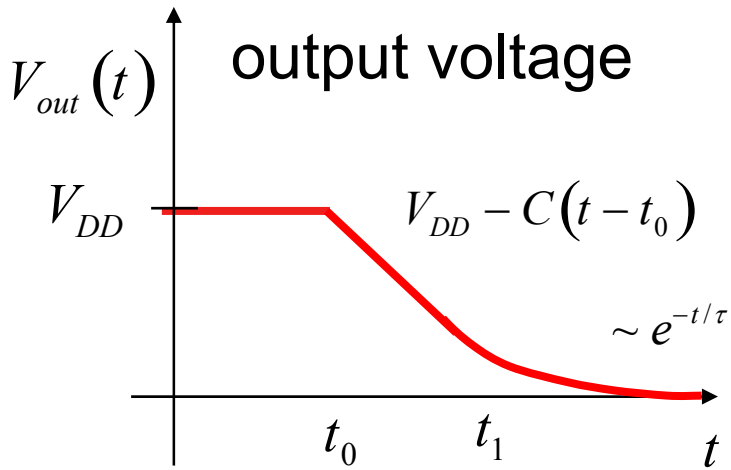
4) **Speed**

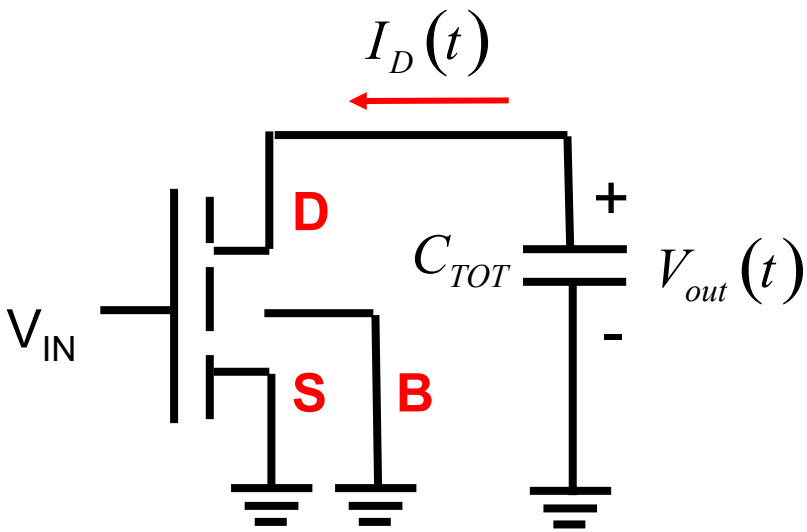
CMOS inverter





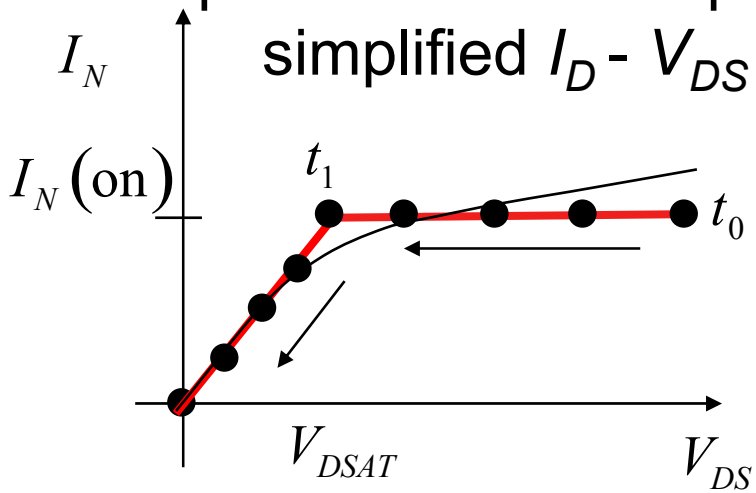


discharging time



quasi-static assumption

simplified I_D - V_{DS}



$$I_d(t) = -C_{TOT}\frac{dV_{out}(t)}{dt}$$

$$V_{out}(t) = V_{DD} - \frac{I_N(\text{on})}{C_T}(t - t_0)$$

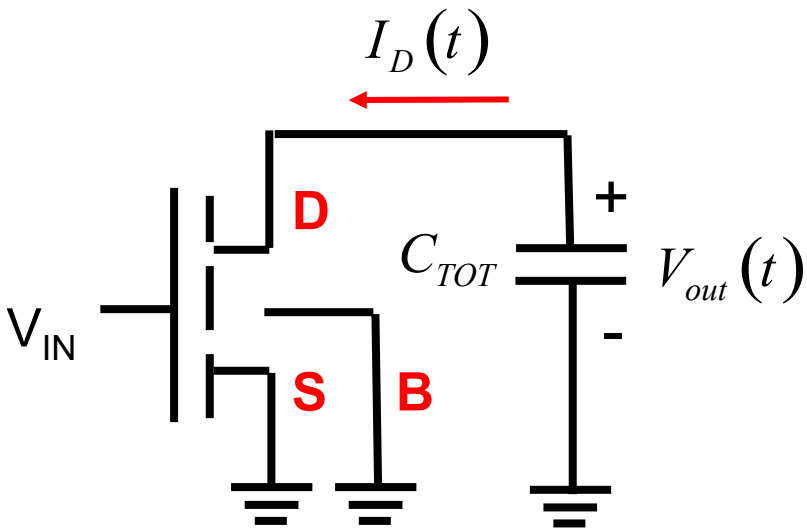
$$t_0 < t < t_1$$

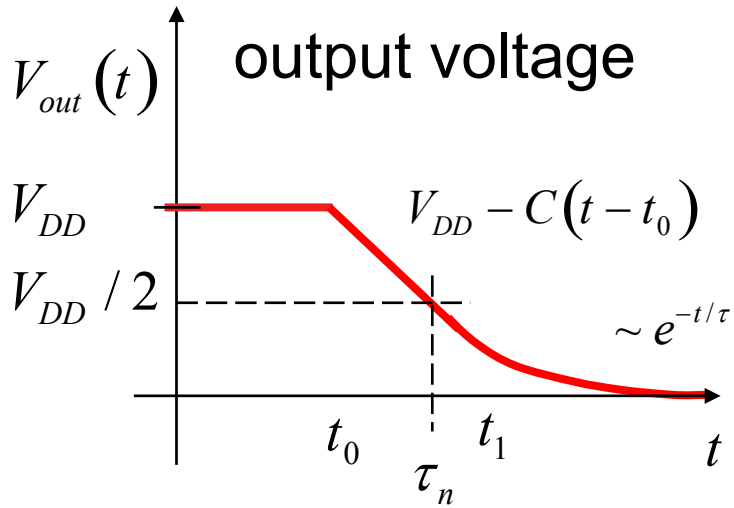
$$\tau = R_{CH}C_{TOT} \qquad R_{CH} = V_{DSAT} / I_N(\text{on})$$

$$V_{out}(t) = V_{out}(t_1)e^{-t/\tau}$$

$$t_0 < t < t_1$$

propagation delay (H-L)





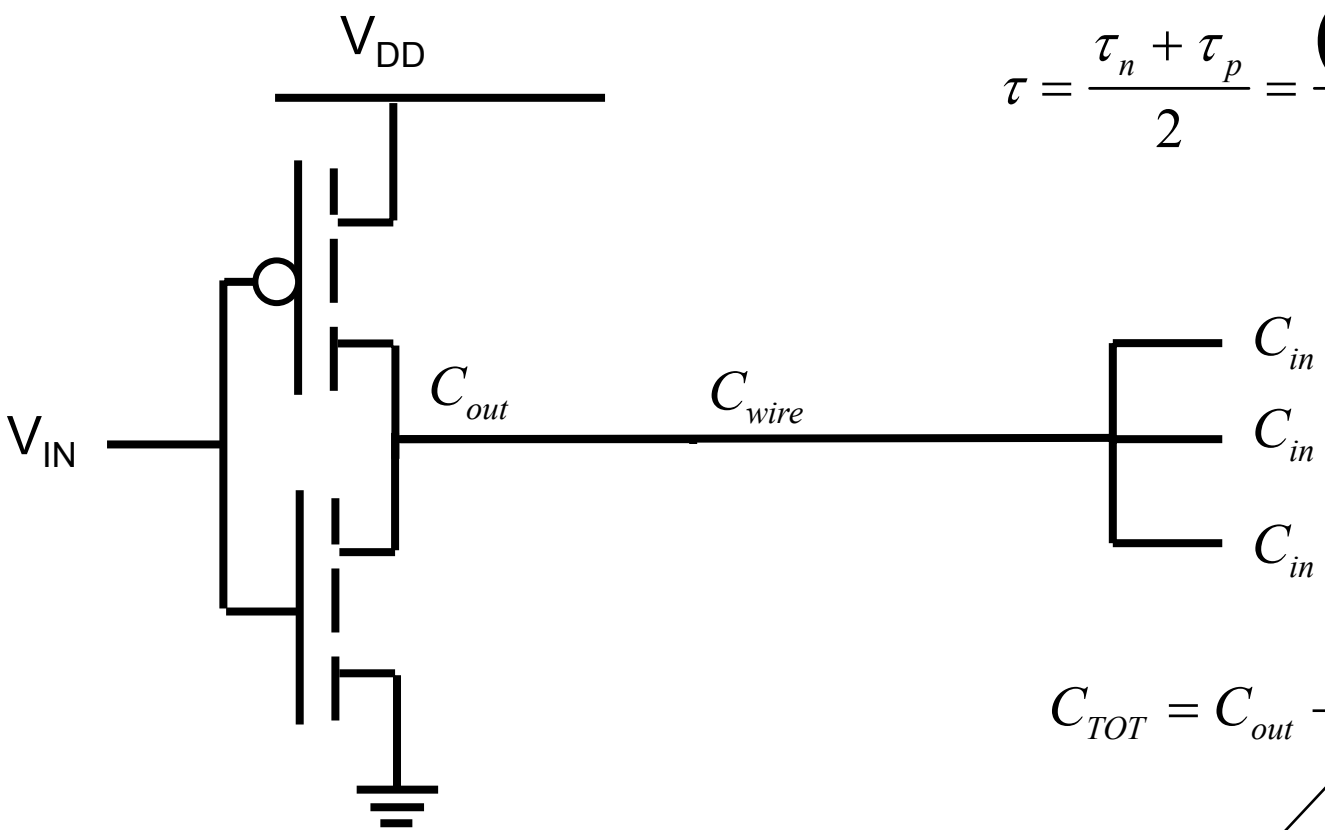
$$V_{out}(t) = V_{DD} - \frac{I_N(\text{on})}{C_T}(t - t_0) \quad t_0 < t < t_1$$

$$V_{DD}/2 = V_{DD} - \frac{I_N(\text{on})}{C_{TOT}}\tau_n$$

$$\tau_n = \frac{C_{TOT}V_{DD}}{2I_N(\text{on})} \equiv R_{swn}C_{TOT}$$

$$R_{swn} = k_n\frac{V_{DD}}{I_N(\text{on})} \qquad k_n = \frac{1}{2}$$

loaded propagation delay

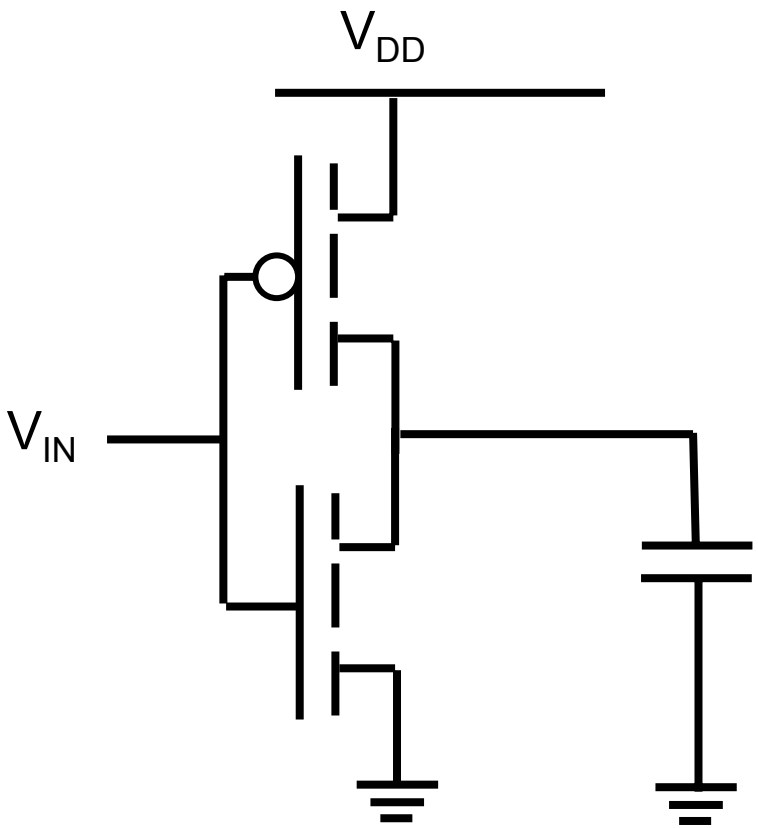


$$\tau = \frac{\tau_n + \tau_p}{2} = \frac{\left(R_{swn} + R_{swp}\right)}{2} C_{TOT}$$

$$C_{TOT} = C_{out} + C_L + FO \times C_{in}$$

interconnect *C*

use of buffers

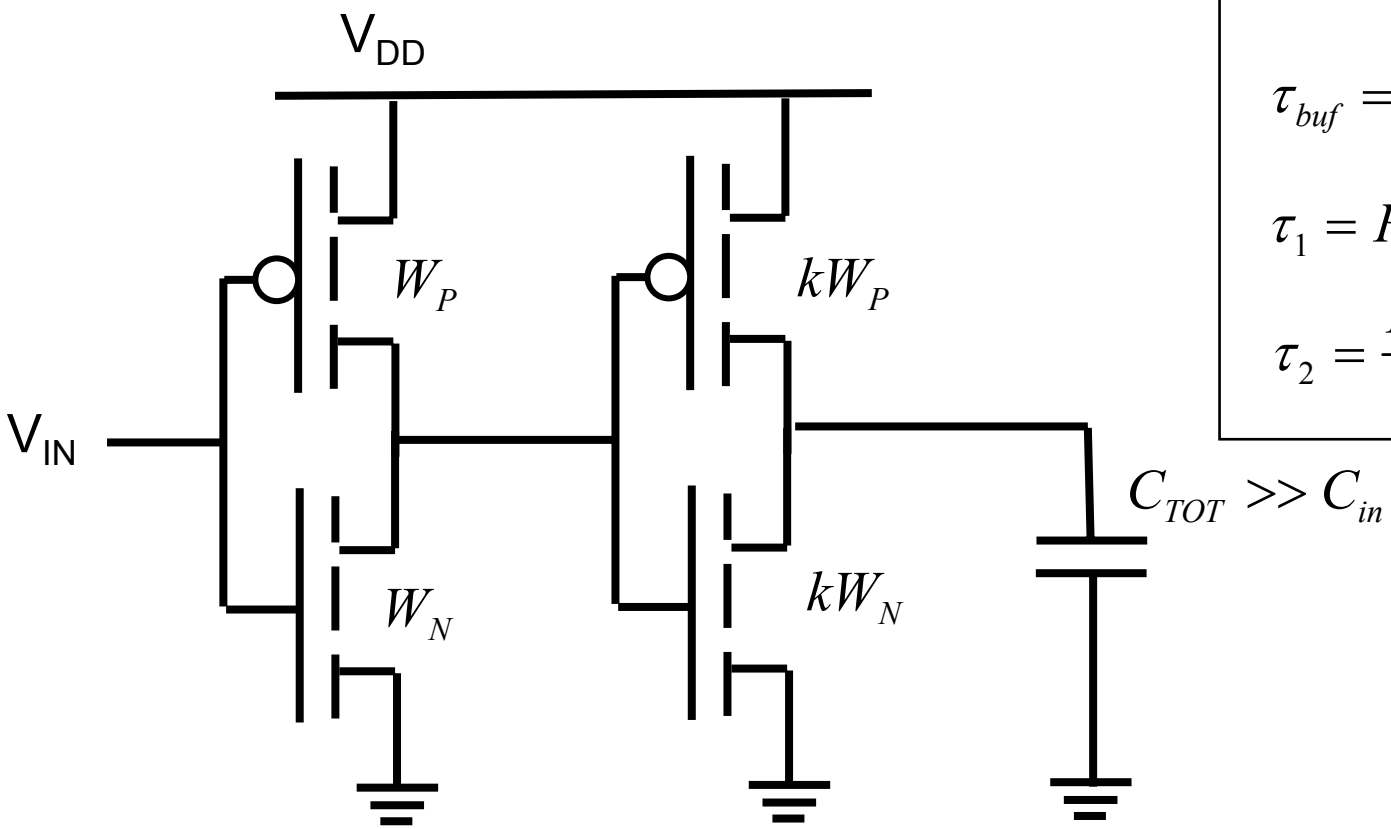


$$C_{TOT} >> C_{in}$$

$$\tau = R_{sw}\left(C_{out} + C_L\right)$$

Can we do better?

delay with buffers



$$\tau = R_{sw}\left(C_{out} + C_L\right)$$

$$\tau_{buf} = \tau_1 + \tau_2$$

$$\tau_1 = R_{sw}\left(C_{out} + kC_{in2}\right)$$

$$\tau_2 = \frac{R_{sw}}{k}\left(kC_{out} + C_L\right)$$

delay with buffers (ii)

$$\tau = R_{sw}\left(C_{out} + C_L\right)$$

$$\tau_{buf} = \tau_1 + \tau_2$$

$$\tau_1 = R_{sw}\left(C_{out} + kC_{in2}\right)$$

$$\tau_2 = \frac{R_{sw}}{k}\left(kC_{out} + C_L\right)$$

$$\tau_{buf} = R_{sw}\left(C_{out} + kC_{in}\right) + \frac{R_{sw}}{k}\left(kC_{out} + C_L\right)$$

$$\tau_{buf} = R_{sw}\left(2C_{out} + kC_{in} + \frac{C_L}{k}\right)$$

$$\frac{d\tau_{buf}}{dk} = 0 \Rightarrow k_{\min} = \sqrt{\frac{C_L}{C_{in}}}$$

$$\tau_{buf}(\min) = R_{sw}\left(2C_{out} + 2\sqrt{C_{in}C_L}\right)$$

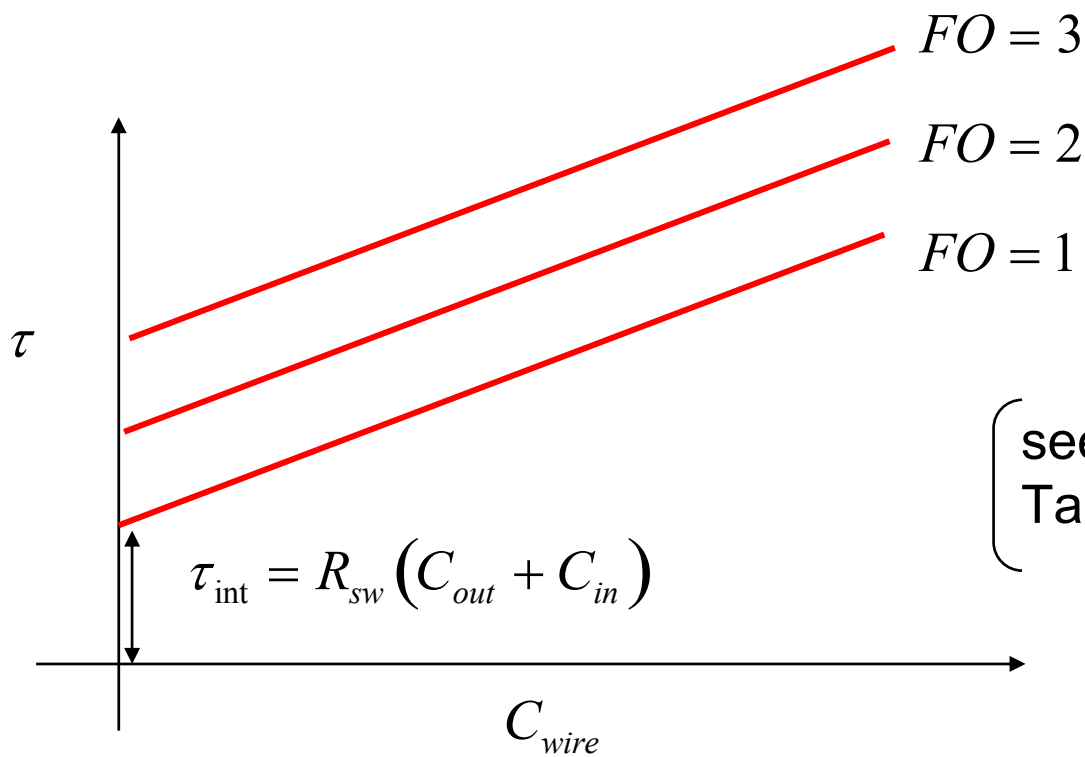
$$C_L >> C_{in}, C_{out}$$

$$\tau_{buf}/\tau = 2\sqrt{C_{in}/C_L} << 1$$

For very heavy loads, use multi-stage buffers.
See Taur and Ning, HW probs. 5.7 - 5.10

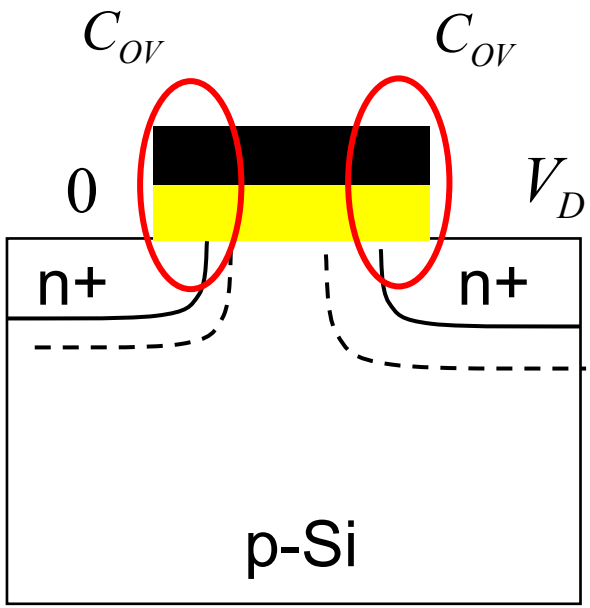
delay vs. load *C*

$$\tau = \frac{\left(R_{swn} + R_{swp}\right)}{2} C_{TOT} = R_{sw}\left(C_{out} + FO \times C_{in} + C_{wire}\right)$$



see Fig. 5.29
Taur and Ning

C_{in} and C_{out}

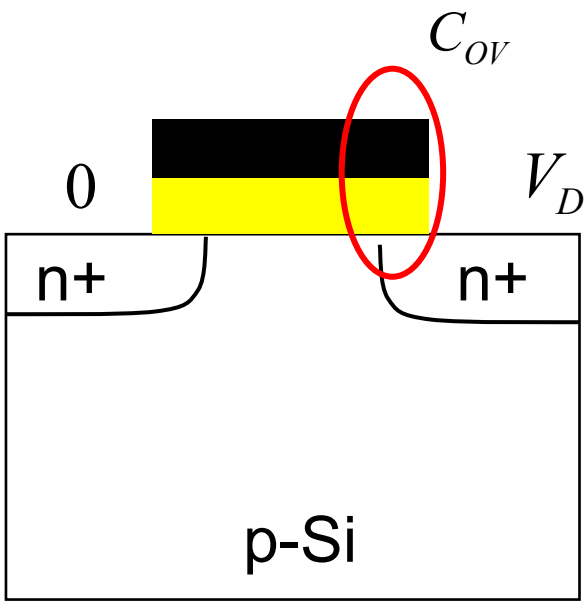


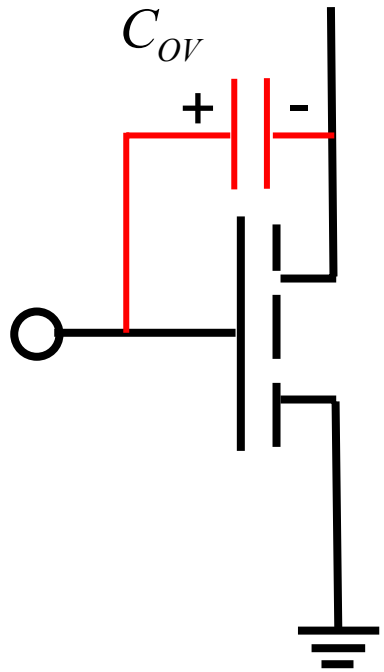
$$C_{in} = \left[C_G + C_{OV} + C_{OV}\right]_N + \left[C_G + C_{OV} + C_{OV}\right]_P$$

$$C_{GN} = C_{OX} W_N L$$

$$C_{out} = \left[C_J + C_{OV}\right]_N + \left[C_J + C_{OV}\right]_P$$

Miller C





capacitors connected between input and output require a special treatment

Outline

1) Review
2) CMOS cirsuits
3) The CMOS inverter
4) Speed

to be continued……