

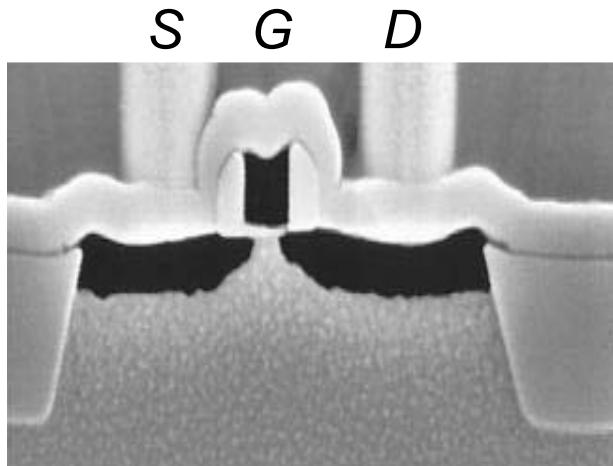
# **EE-612:**

# **Lecture 1: MOSFET Review**

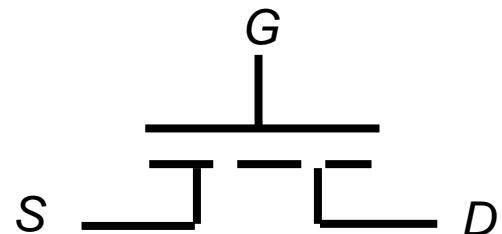
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Electrical and Computer Engineering  
Purdue University  
West Lafayette, IN USA  
Fall 2006

# MOSFETs

physical structure



circuit schematic



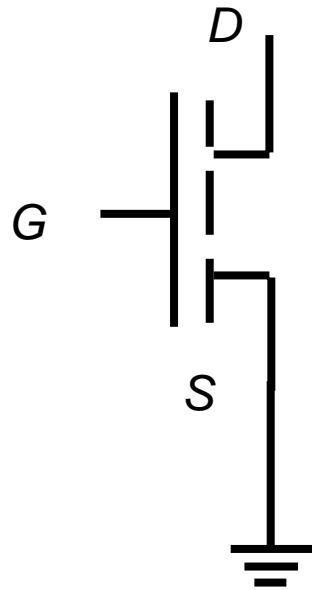
65 nm technology node:

$$L = 35 \text{ nm}$$

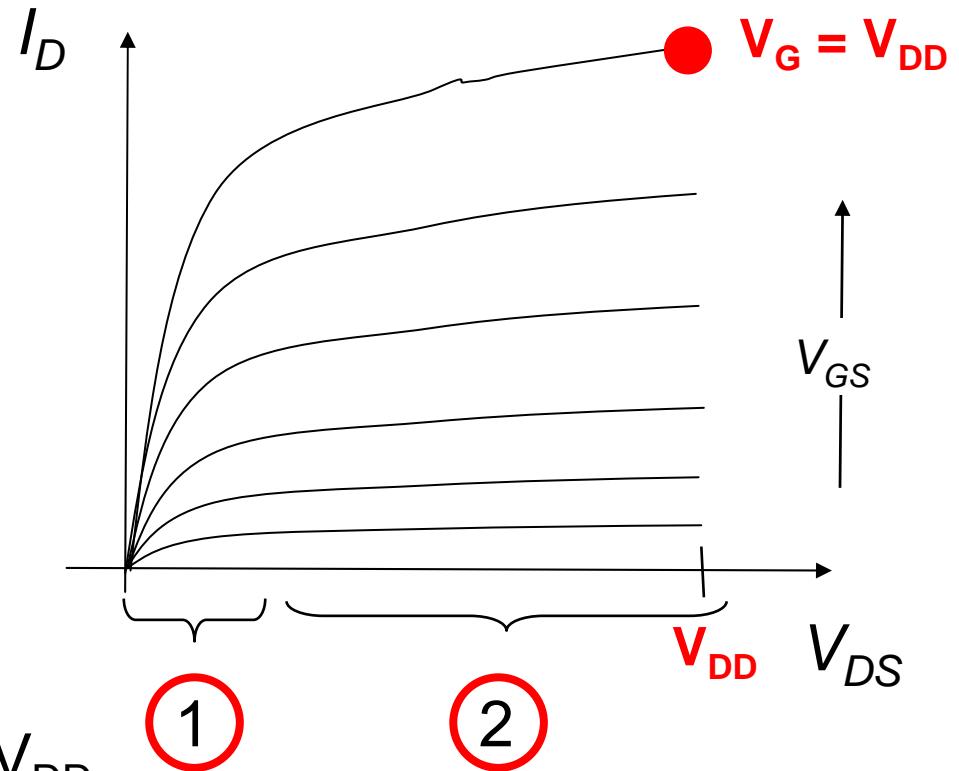
$$T_{ox} = 1.2 \text{ nm}$$

$$V_{DD} = 1.2 \text{ V}$$

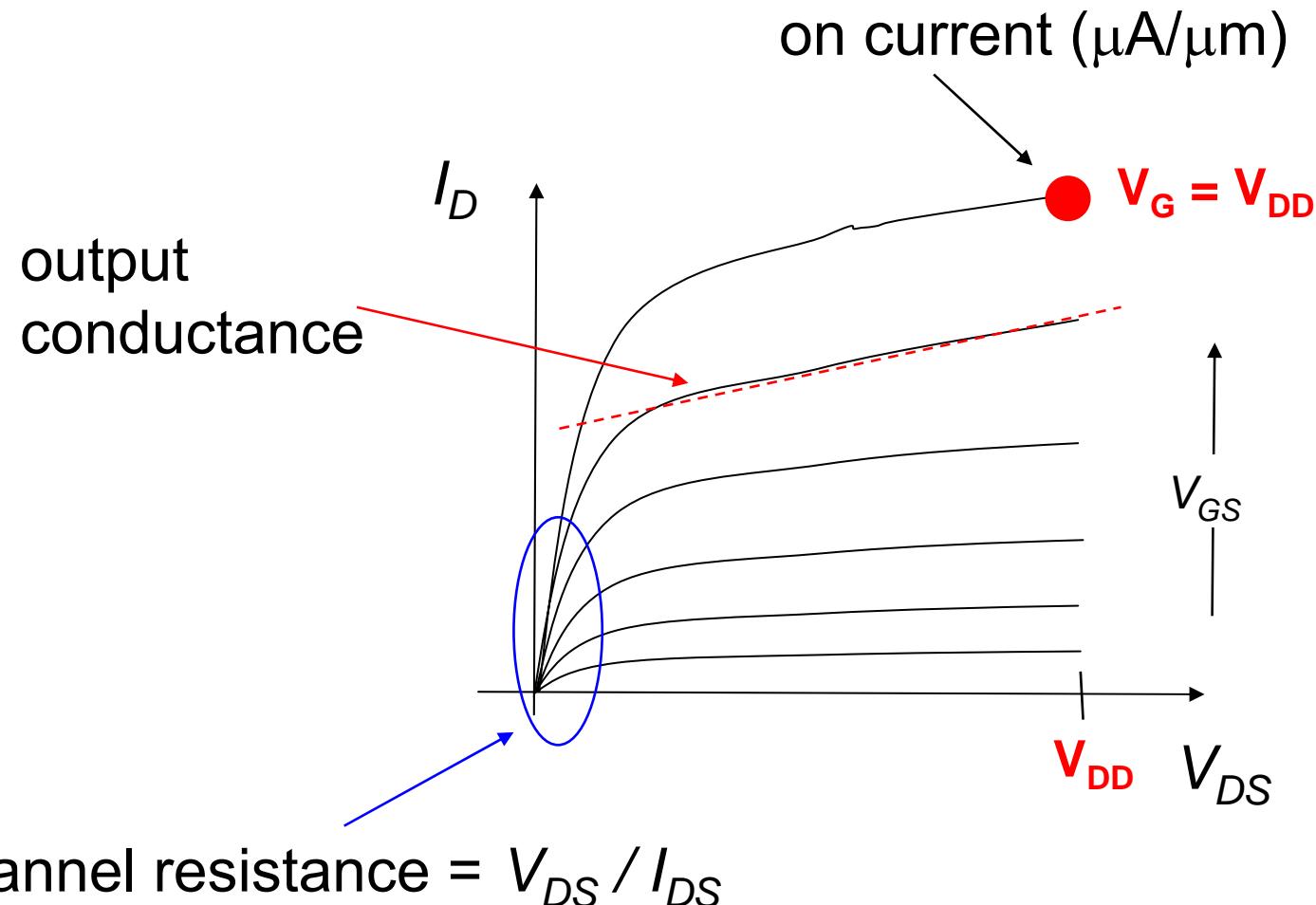
# common source characteristics



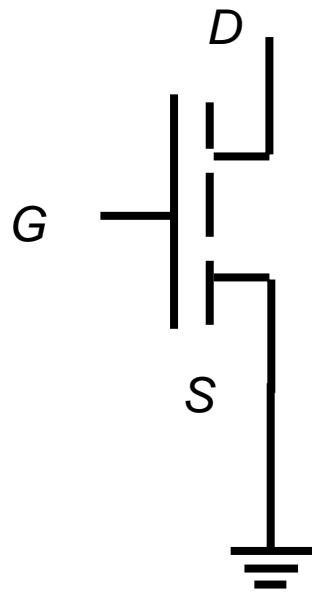
- 1) ground source
- 2) set  $V_G$
- 3) sweep  $V_D$  from 0 to  $V_{DD}$
- 4) Step  $V_G$  from 0 to  $V_{DD}$



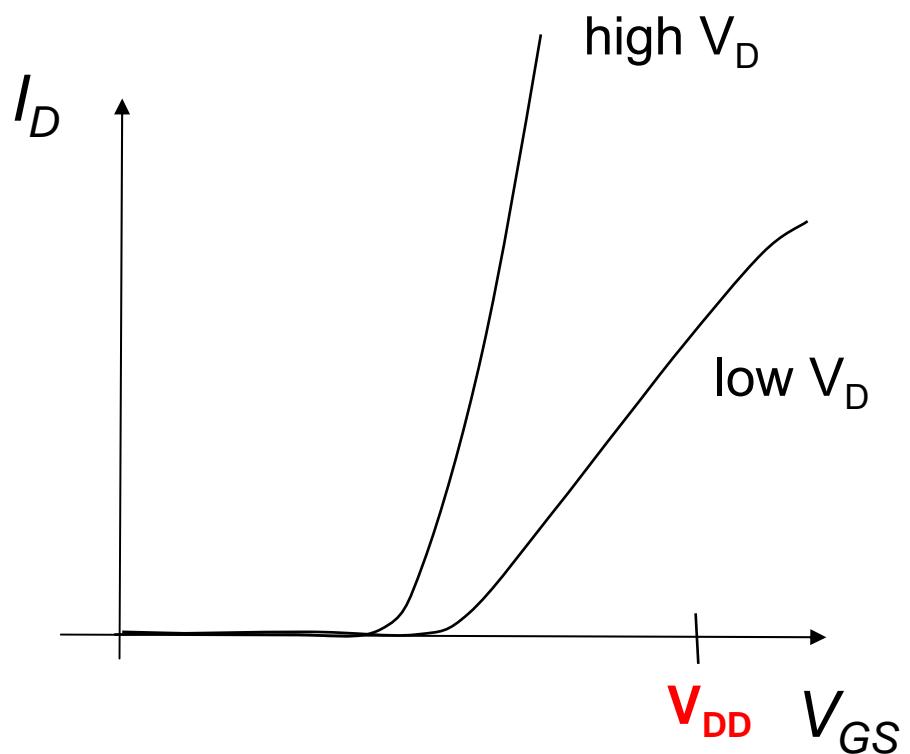
# common source characteristics



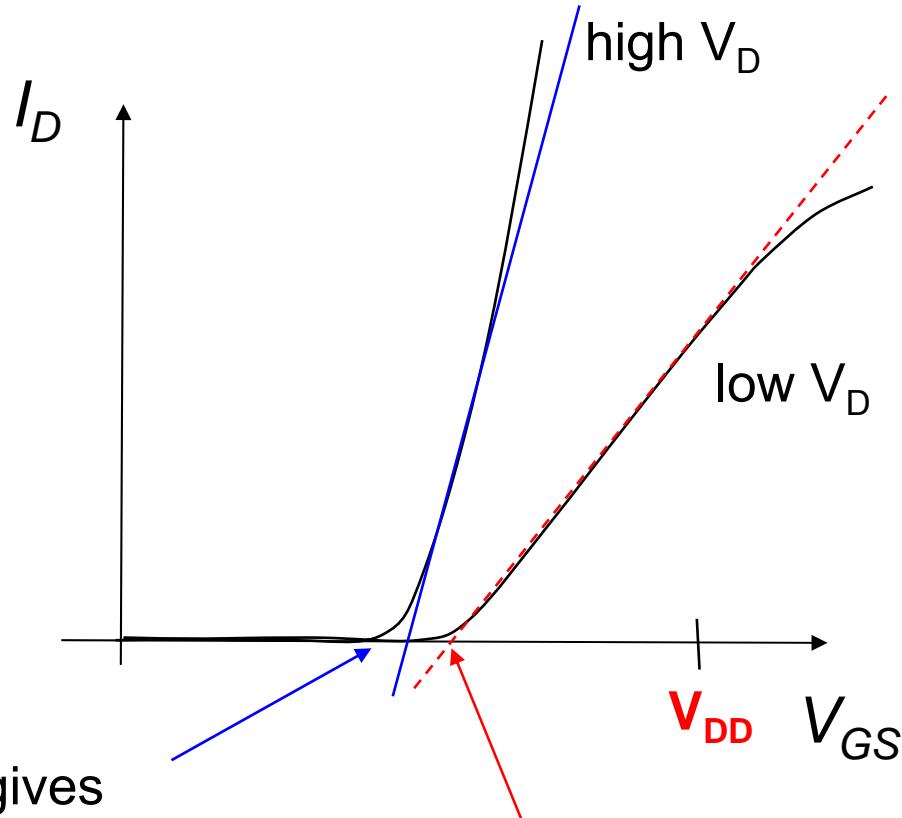
# transfer characteristics



- 1) ground source
- 2) set  $V_D$
- 3) sweep  $V_G$  from 0 to  $V_{DD}$



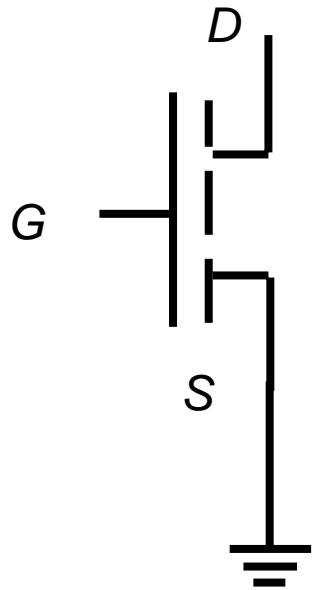
# transfer characteristics



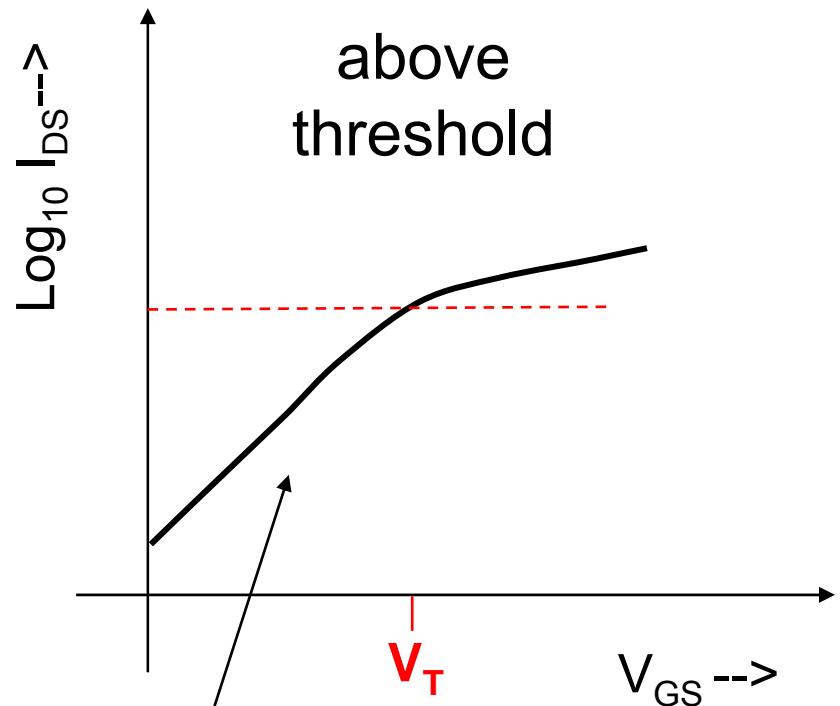
intercept gives  
 $V_T(\text{sat}) < V_T(\text{lin})$

intercept gives  $V_T(\text{lin})$   
slope is related to the effective mobility

# $\log_{10} I_D$ vs. $V_{GS}$

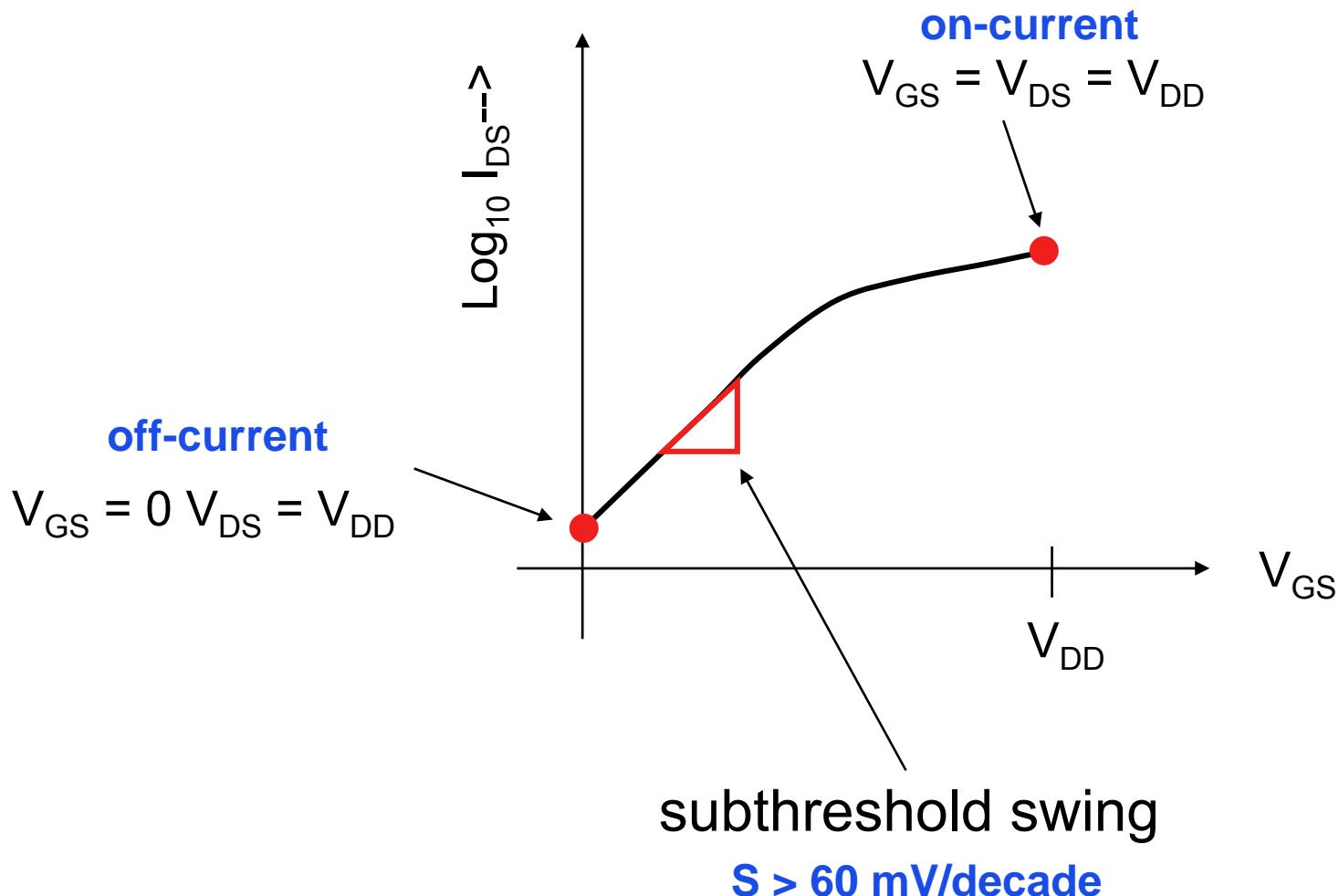


- 1) ground source
- 2) set  $V_D = V_{DD}$
- 3) sweep  $V_G$  from 0 to  $V_{DD}$

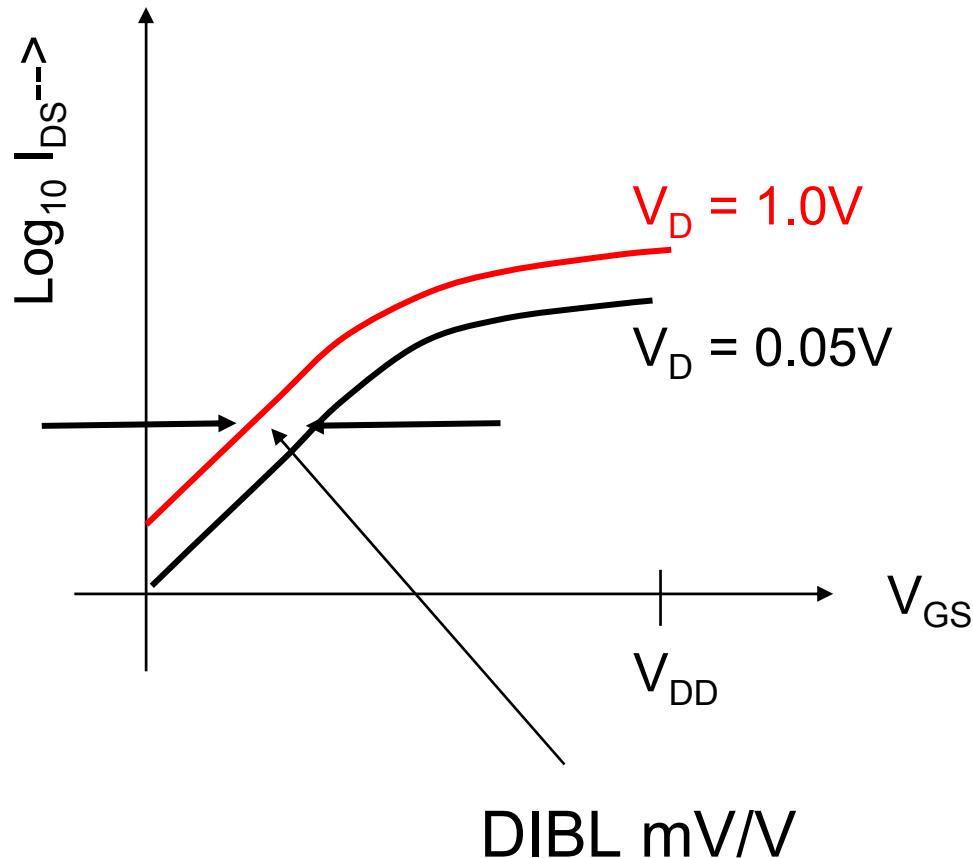


*subthreshold  
region*

# $\log_{10} I_D$ vs. $V_{GS}$

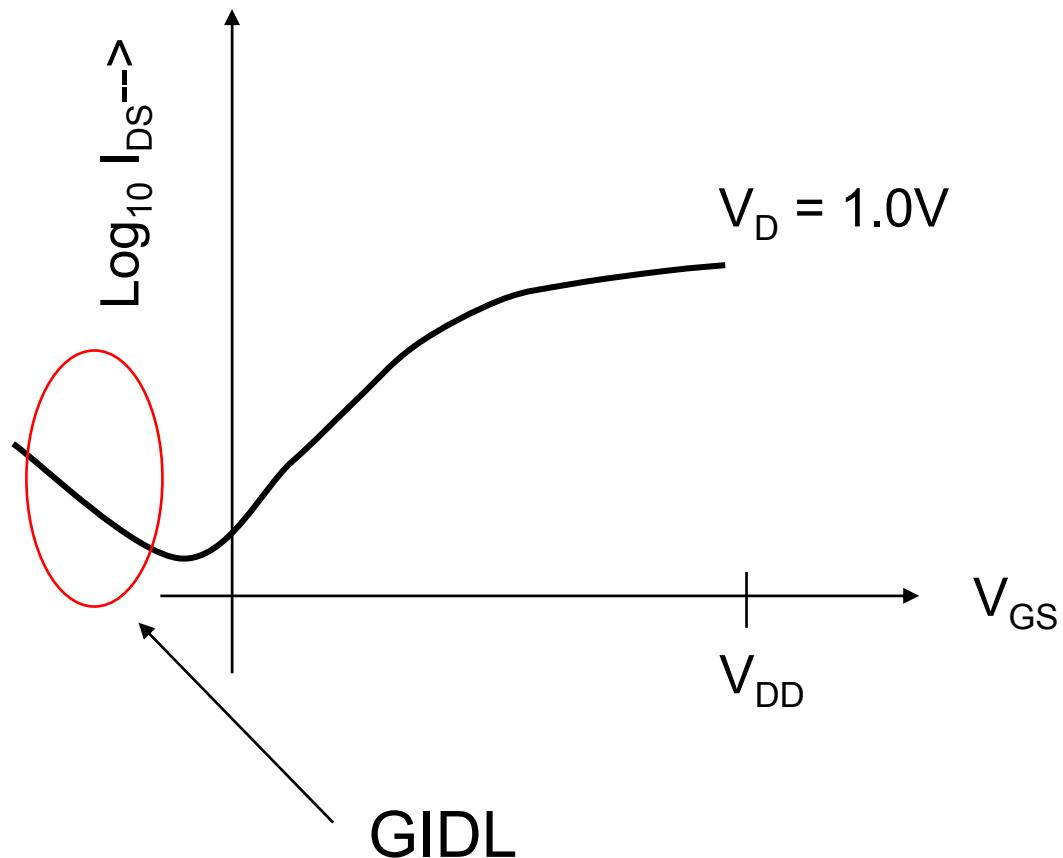


# DIBL (drain-induced barrier lowering)

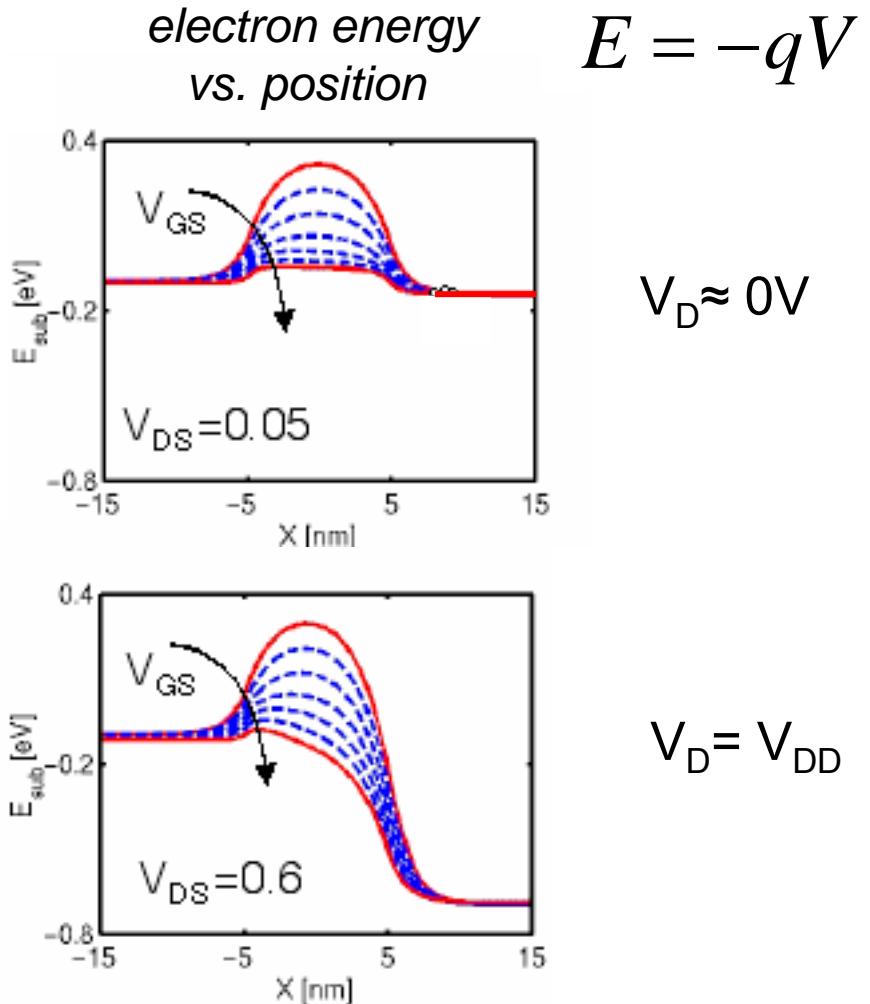
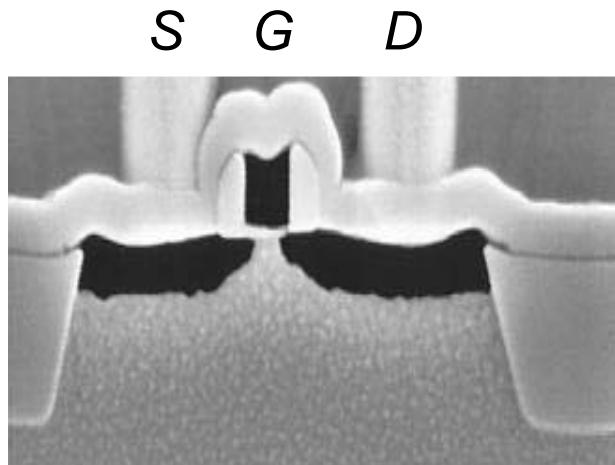


$$V_T(V_D = 1.0V) < V_T(V_D = 0.05V)$$

# GIDL (gate-induced drain leakage)

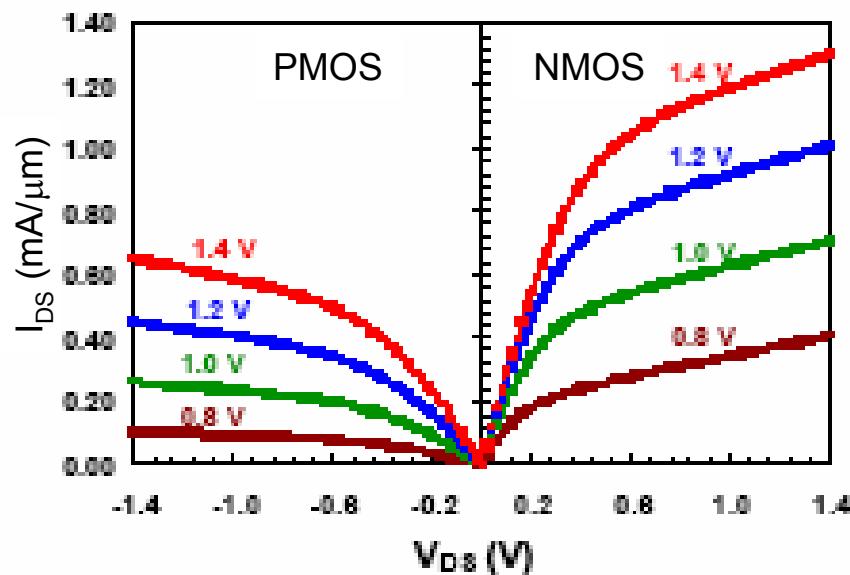


# physics of MOSFETs



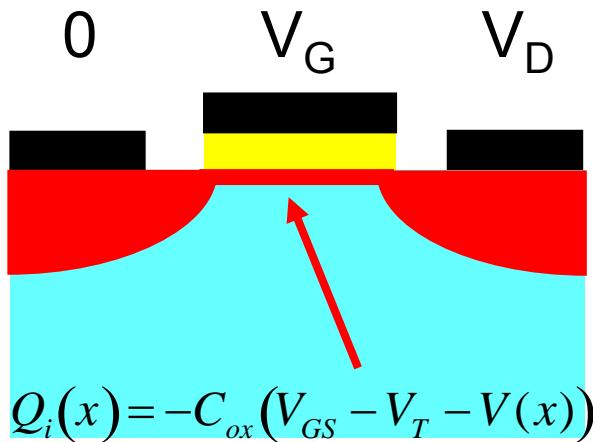
# modern MOSFETs

130 nm technology ( $L_G = 60 \text{ nm}$ )



Intel Technical J., Vol. 6, May 16, 2002.  
(low  $V_T$  device)

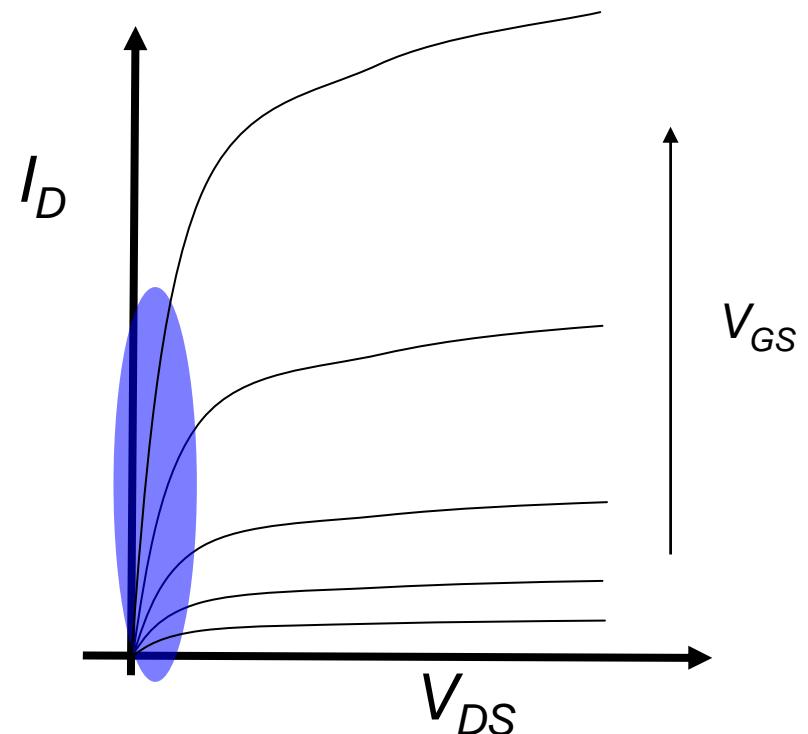
# MOSFET IV: low $V_{DS}$



$$I_D = W Q_i(x) v_x(x) = W Q_i(0) v_x(0)$$

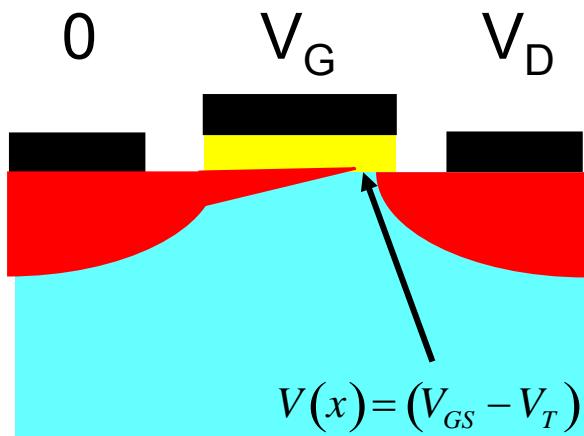
$$I_D = W C_{ox} (V_{GS} - V_T) \mu_{eff} E_x$$

$$E_x = \frac{V_{DS}}{L}$$



$$I_D = \frac{W}{L} \mu_{eff} C_{ox} (V_{GS} - V_T) V_{DS}$$

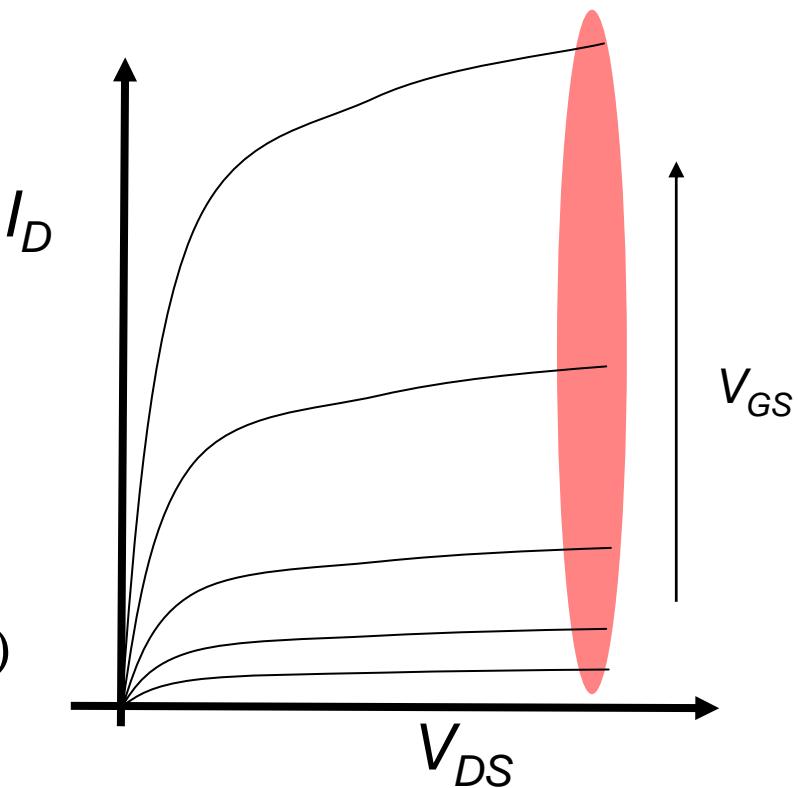
# MOSFET IV: high $V_{DS}$



$$I_D = W Q_i(x) v_x(x) = W Q_i(0) v_x(0)$$

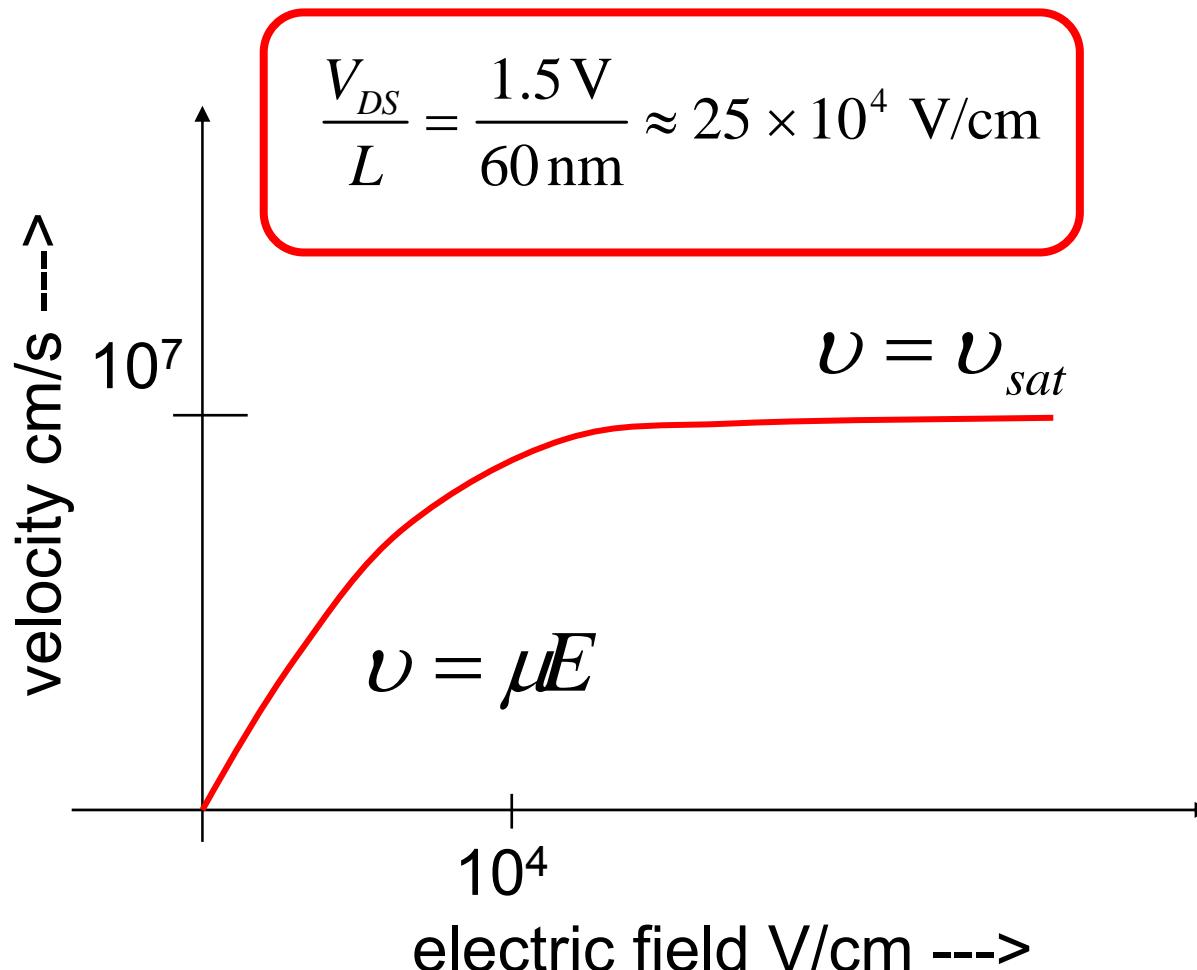
$$I_D = W C_{ox} (V_{GS} - V_T) \mu_{eff} E_x$$

$$E_x \approx \frac{V_{GS} - V_T}{L}$$

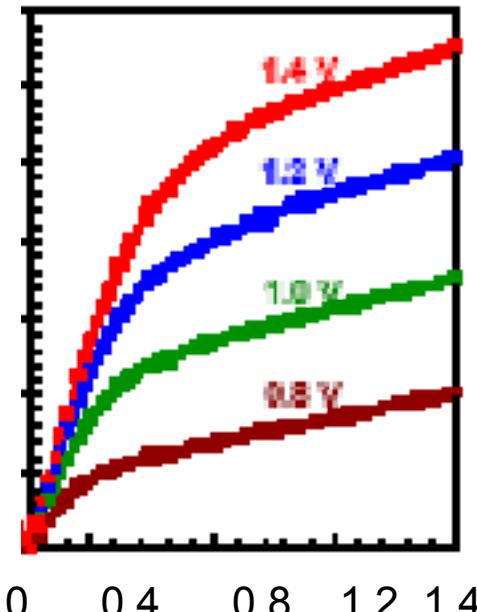
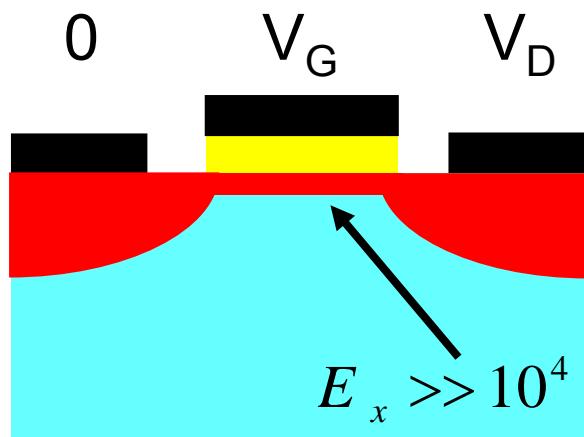


$$I_D = \frac{W}{2L} \mu_{eff} C_{ox} (V_{GS} - V_T)^2$$

# velocity saturation



# MOSFET IV: velocity saturation



$$I_D = W Q_i(x) v_x(x) = W Q_i(0) v_x(0)$$

$$I_D = W C_{ox} (V_{GS} - V_T) v_{sat}$$

$$I_D = W C_{ox} v_{sat} (V_{GS} - V_T)$$

# MOSFET IV: discussion

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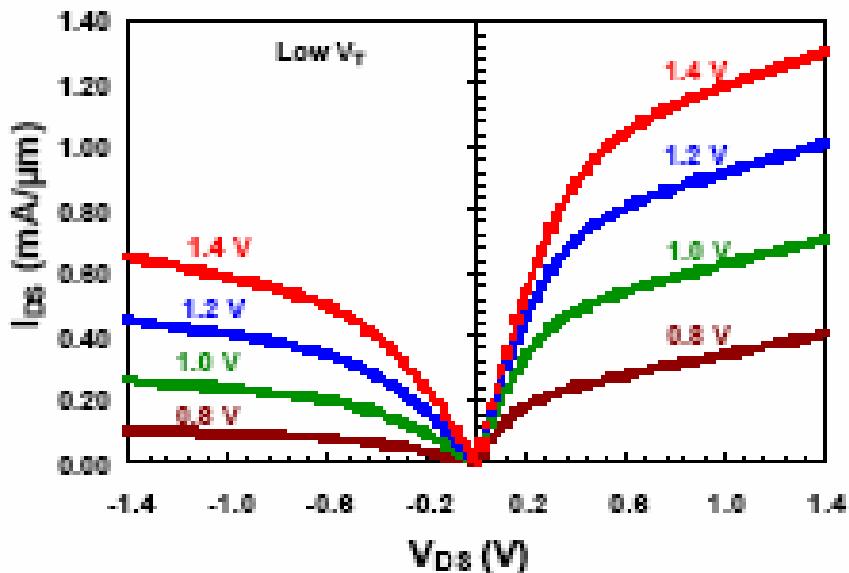
$$Q_i = -C_{ox}(V_{GS} - V_T) \approx ?$$

$$\left. \begin{array}{l} V_{GS} = 1.2V \\ V_T = 0.3V \\ T_{ox} = 1.5 \text{ nm} \end{array} \right\} |Q_i| \approx 2 \times 10^{-6} \text{ C/cm}^2$$

$$\frac{|Q_i|}{q} \approx 1 \times 10^{13} / \text{cm}^2$$

# MOSFET IV: discussion

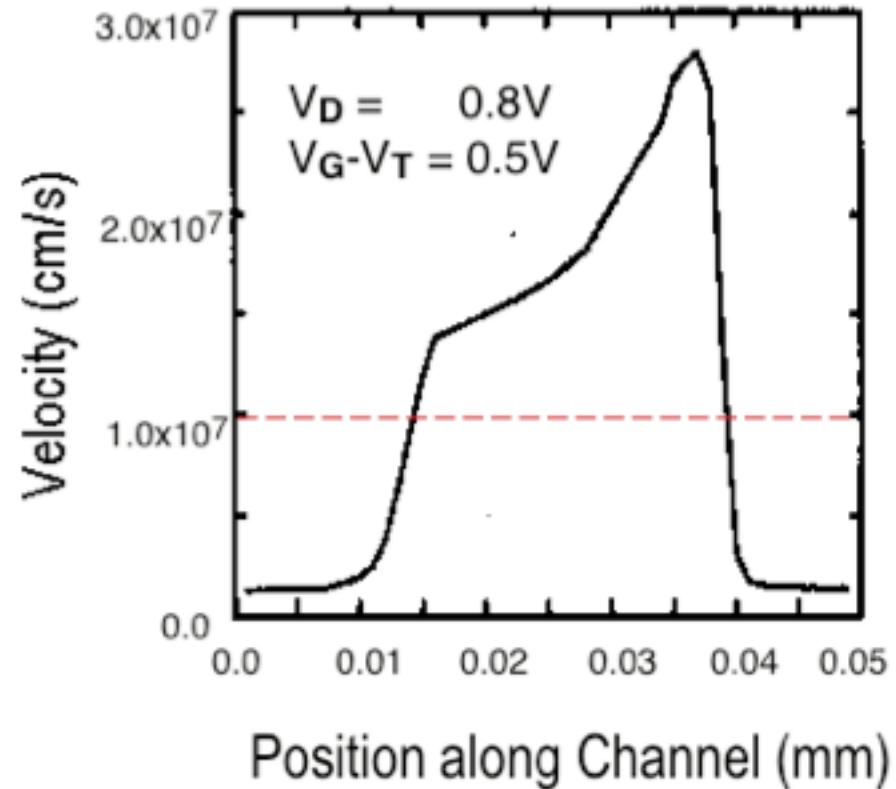
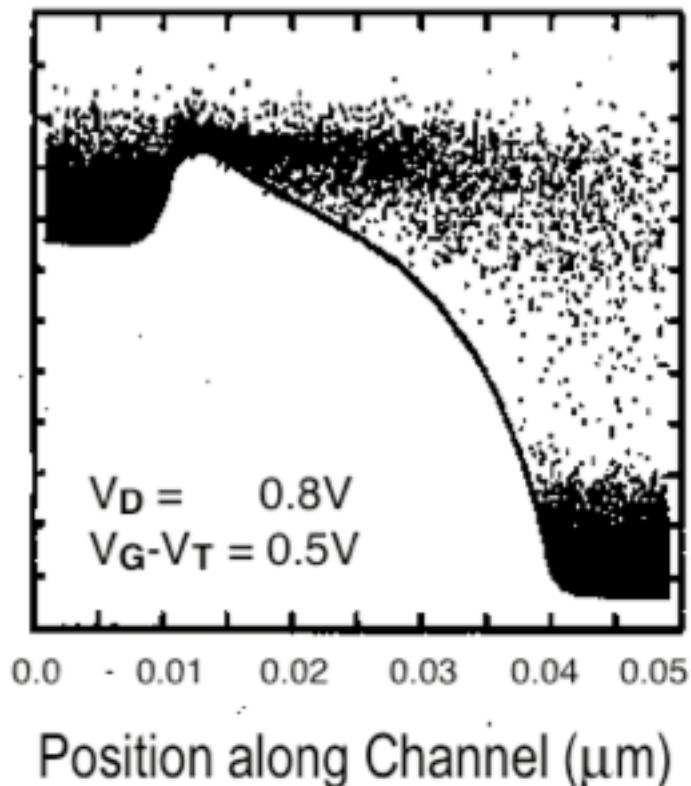
130 nm technology ( $L_G = 60 \text{ nm}$ )



$$I_D \approx W Q_i(0) v_{sat} \approx 1.6 \text{ mA}/\mu\text{m}$$

Intel Technical J., Vol. 6, May 16, 2002.

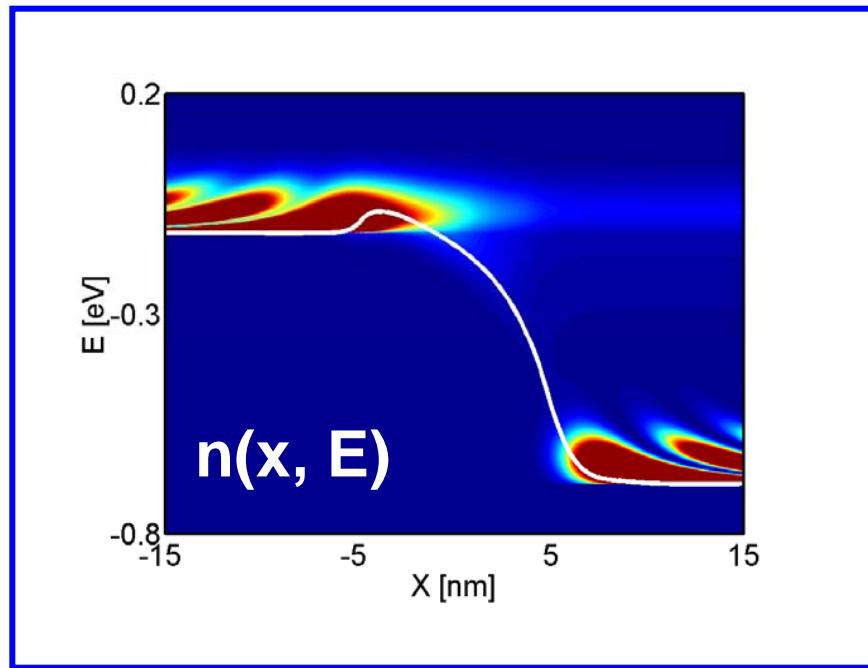
# MOSFET IV: velocity overshoot



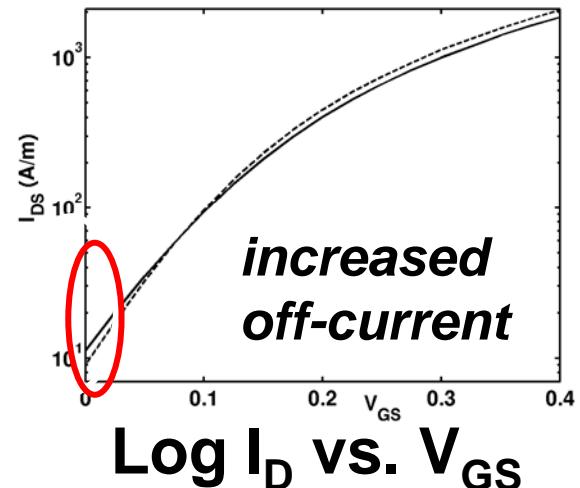
Frank, Laux, and Fischetti, IEDM Tech. Dig., p. 553, 1992

# MOSFET IV: Quantum effects

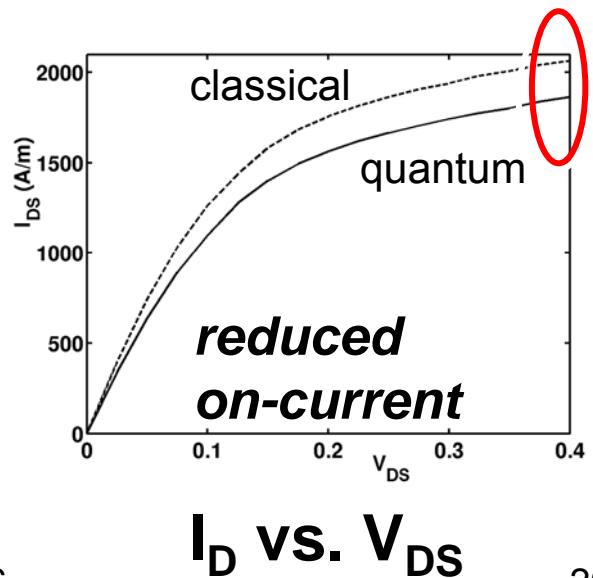
$L = 10 \text{ nm}$



(quantum confinement  
treated in both cases)



**Log  $I_D$  vs.  $V_{GS}$**



**$I_D$  vs.  $V_{DS}$**

nanoMOS at [www.nanohub.org](http://www.nanohub.org)

# Summary

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- 1) A MOSFET's  $I_D$  = inversion layer charge times velocity
- 2) 2D electrostatics determine  $Q_i$
- 3) *Carrier transport determines the velocity*
- 4) *Second order effects are becoming first order  
(e.g. leakage)*