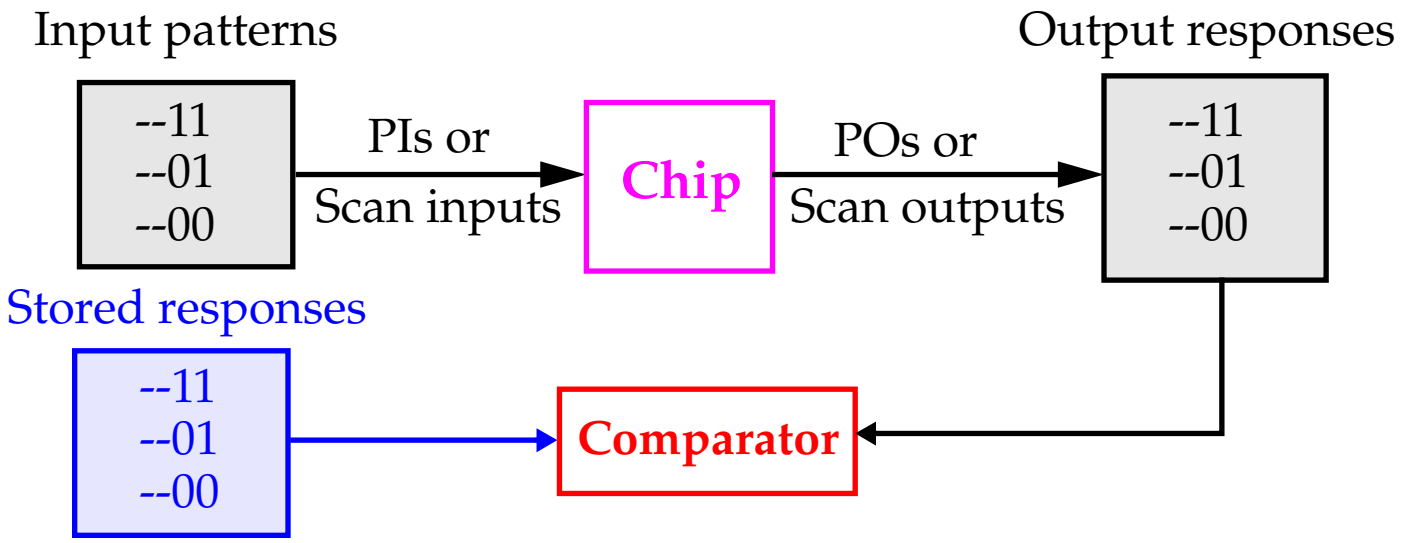
Testing Principles



When the chip is digital, the stimuli are called **test patterns** or **test vectors**.

Automatic test equipment (ATE) carries out this process.

A powerful computer operating under the control of a **test program**, a program written in a high level language.

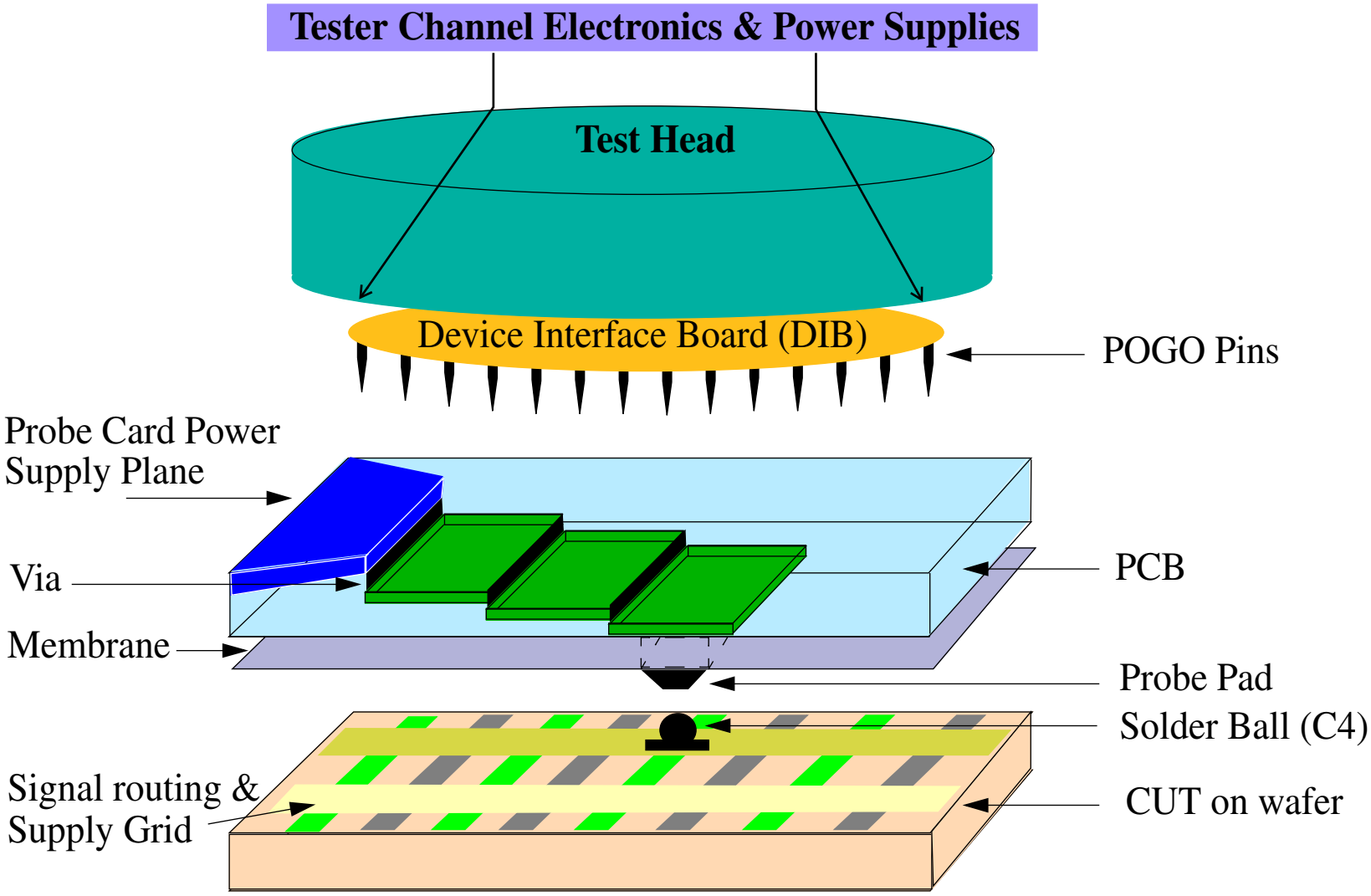
Chips are automatically fed to the tester through the wafer handler system.

A *probe card* or *membrane probe* contacts pads of the dies on the wafer.

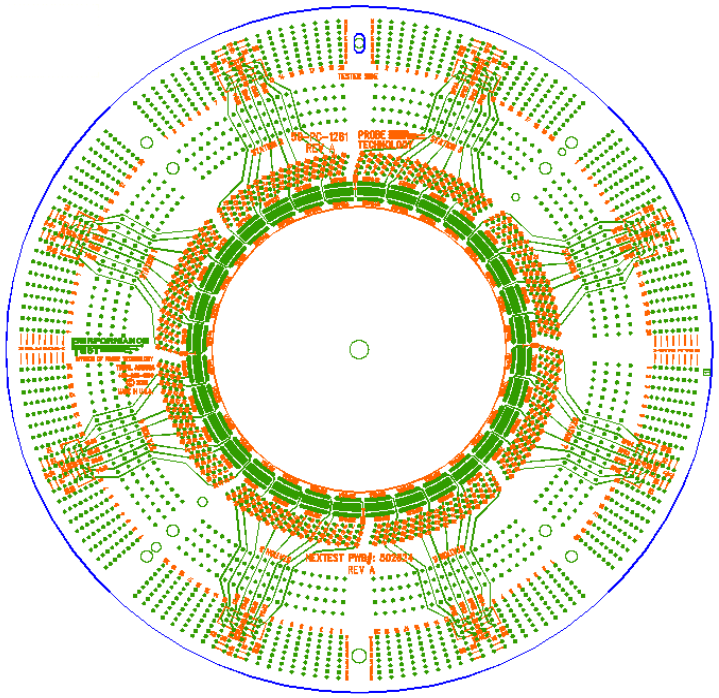
ATE for Manufacturing Test

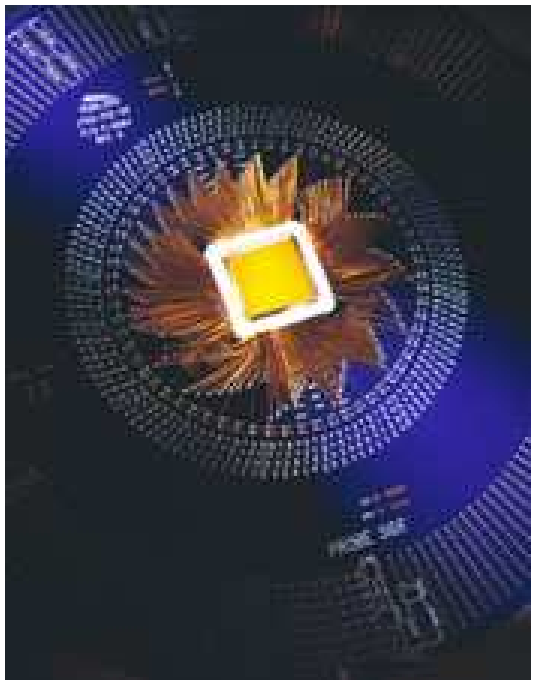
Wafer Probe Physical Model

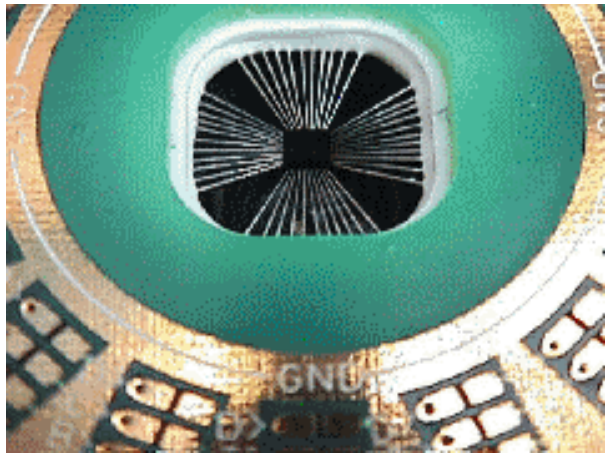
Test head and membrane (cobra) probe card for probing C4s.



Cantilever Style Probe Cards



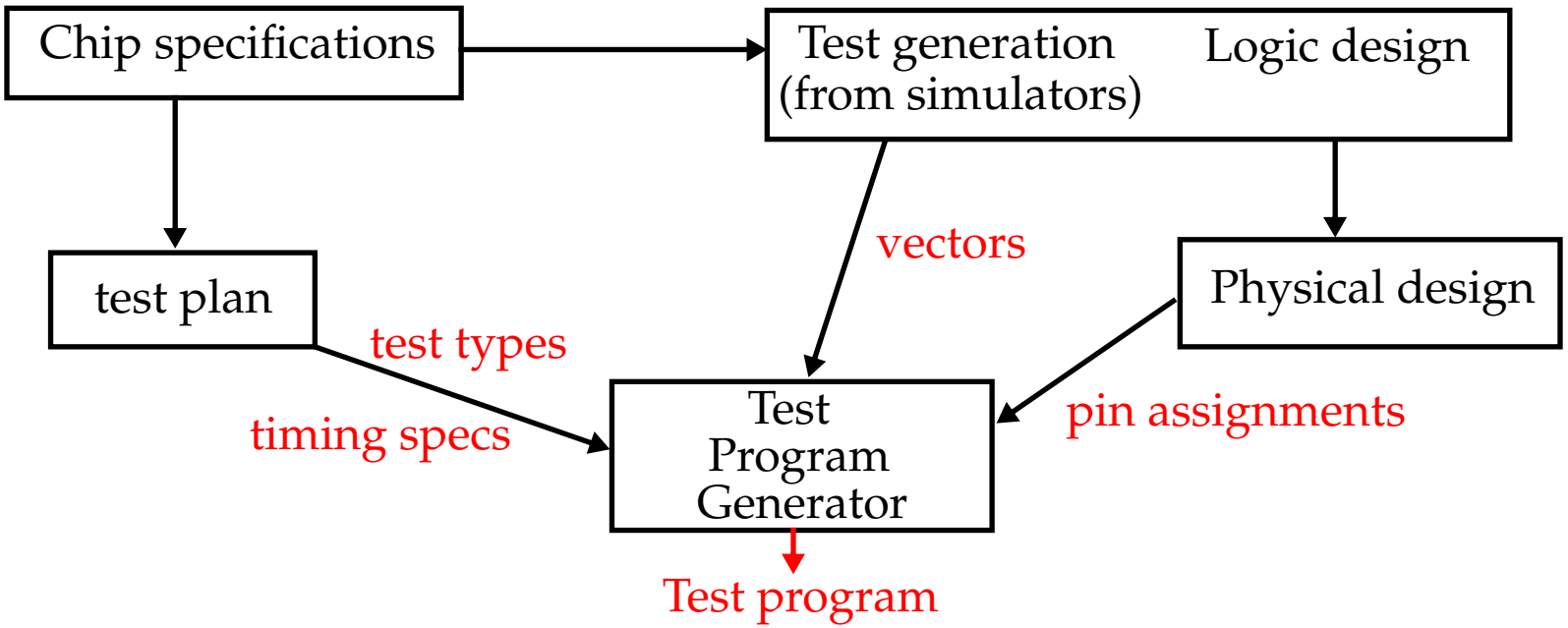




Test Programming

The test program and test vectors are needed once the chip is contacted.

CAD tools used to automate the generation of the test programs.



3 main purposes of the ATE test data:

- Accept/reject the chip-under-test (CUT).
- Provides information about the fabrication process (yield learning).
- Provides information about design weaknesses (debug).

4 Basic Types of Testing

Characterization testing, design debug or verification testing:

Verifies correctness of design and test procedure.

Production (**go/no-go test**):

Factory testing of all manufactured chips for parametric faults and for random defects.

Burn-in or stress test:

Testing designed to stress the chip and accelerate the mechanisms that cause the chip to fail.

Acceptance testing or incoming inspection:

Customer performs tests on purchased parts to ensure quality.

Types of Testing

- Characterization testing, design debug or verification testing

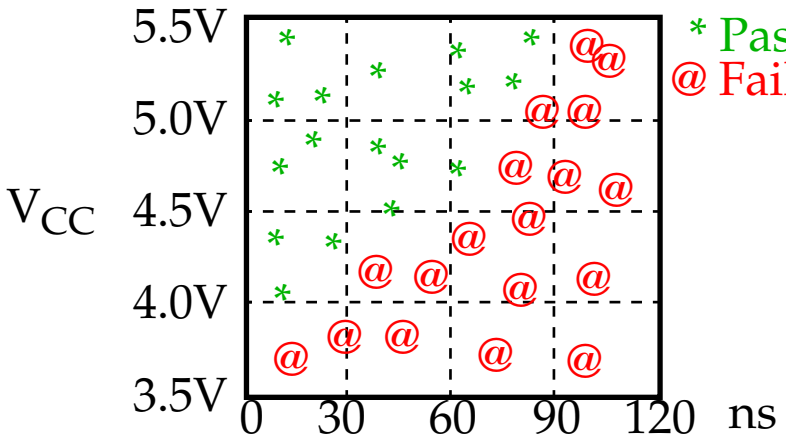
  Performed on new designs -- determines if design is correct and meets ALL specifications -- labor intensive.

  AC, DC and functional tests performed.

  Probing of internal chip nodes may also be performed.

  Specialized tools are used, such as scanning electron microscopes (SEM) and electron beam tests.

  Focus on worst case corners. *Shmoo plots* are created.



Statistically significant number of chips are chosen.

Repeated for all 2+ environment variables.

Types of Testing

- Characterization testing, design debug or verification testing

  The process is designed to (1) *diagnose* and *correct* errors, (2) set the final specifications and (3) is used to develop a production test program.

  Less intensive characterization test performed during normal life-cycle of chip to improve design and process yield.

  Yield: Fraction of acceptable parts among all fabricated parts.

- Production (go/no-go test)

  Shorter and less intensive test performed on every chip.

  Enforces quality requirements by determining if chip specs are met.

  Main driver is cost -- test time MUST be minimized.

  Tests must have high coverage of modeled faults.

  No fault diagnosis, only an outgoing inspection test which verifies all relevant specifications.

Types of Testing

- Burn-in or stress test

  Some chips that pass production test will fail very quickly thereafter.

  Burn-in ensures *reliability* by forcing failure in these "weak" chips.

  Key is to **accelerate** the failure mechanisms by increasing temperature and/or voltage while applying test patterns.

  Two types of failures are isolated by burn-in:

  Infant mortality failures:

  Often caused by a combination of sensitive design and process variations.

  Short-term burn-in effective (10-30 hours).

  Freak failures:

  Same failure mechanisms as reliable devices.

  Long burn-in time required (100-1000 hours).

  Very expensive.

Types of Testing

- Incoming Inspection

  System manufacturers perform before incorporating chips into systems.

  Once inserted, the cost of discovery can be much higher than cost of the inspection test.

  The rule of Ten: The cost of discovering a defective chip increases by an order of magnitude at each successive level of integration, from die/package, board and system.

  Can be similar or more comprehensive than production test.

  Incoming inspection can be performed on a random sample of chips.

Types of Tests

- Parametric tests:

  DC parametric tests include shorts test, opens test, leakage test, etc.

  AC parametric tests include delay test, setup and hold test, etc.

- Functional tests:

  Input vectors and corresponding responses designed to check proper operation of a verified design.

  Structural tests that target specific faults on internal nodes of the chip.

  Often achieve high coverage of the modeled faults (>95%).

  Functional vectors, on the other hand, often refer to **verification vectors** designed to determine if hardware matches specification.

  Typically they have low fault coverage (<70%).

Test Flow

The type of test depends of the manufacturing level:

- In-line tests

  Performed during fabrication to monitor the fabrication process.

- Wafer sort or probe test

  Performed before wafer is scribed (cut into chips).

  Test site characterization is also performed during wafer sort.

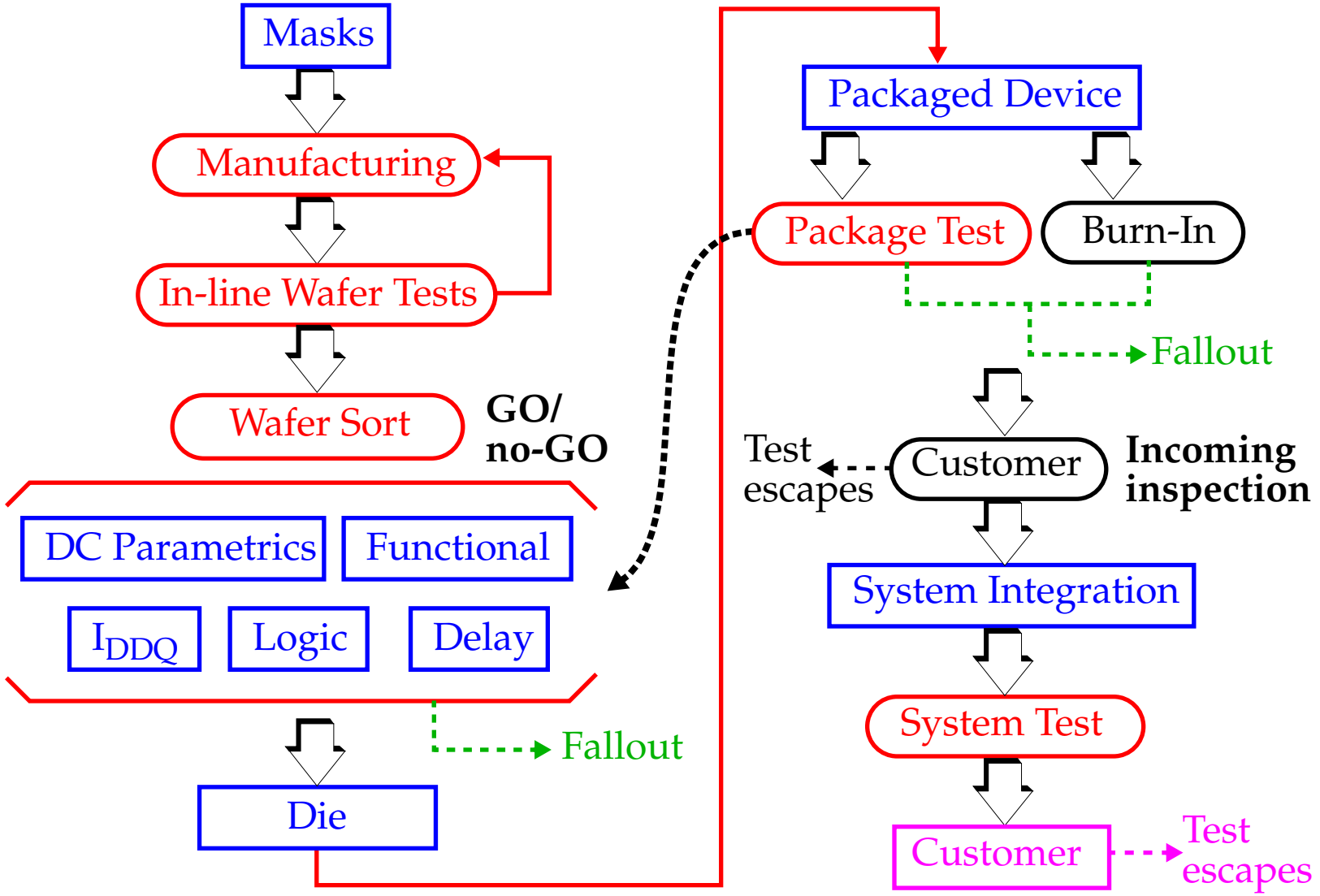
  Test structures are tested to assess characteristics of the technology including gate threshold, poly sheet resistance, etc.

- Packaged device tests

  Production testing performed on packaged parts while inserted into load boards.

  Burn-in typically performed at this stage of manufacturing.

Test Flow


Masks
Manufacturing
In-line Wafer Tests
Wafer Sort
GO/
no-GO
DC Parametrics
Functional
I_{DDQ}
Logic
Delay
Fallout
Die
Packaged Device
Package Test
Burn-In
Fallout
Test
escapes
Customer
Incoming
inspection
System Integration
System Test
Customer
Test
escapes