Department of Computer Science and Electrical Engineering
UMBC
Project Description for CMPE418 (VLSI Design and Verification)

Project Assigned: 04/27/07
Project Due: 05/15/07

Design a 32 bit MAC (Multiply and Accumulate) unit as depicted in the figure.
-Write a verilog RTL code for each part (multiplier, adder and registers).
-Simulate your code to verify its functionality. (a help file is provided for using verilog simulator in Cadence)
-Use Cadence RTL Compiler or BuildGates to synthesize your code to gate level description. (use GSC generic library provided on the web site.)
-Use Cadence SOC Encounter to obtain a layout for the system. Report the maximum clock frequency and slack.
-Redesign the registers to implement BILBO blocks (that can be used as LFSR, MISR, scan register or normal register).
-Write a testbench for the new design that demonstrates scanning in the LFSR seed, performing random pattern generation and response compaction and scanning out the final response.