CMPE 415: Programmable Logic Devices

Course:
CMPE 415: Programmable Logic Devices, Fall 2007

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FPGA Text:
The Design Warrior's Guide to FPGAs, Devices, Tools and Flows, Clive "Max"
Maxfield, ISBN: 0-7506-7604-3
Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Michael D.
Ciletti, ISBN: 0-13-977398-3

Verilog Text:
Advanced Digital Logic Design Using Verilog, State Machines and Synthesis for
FPGAs, Sunggu Lee, ISBN: 0-534-55161-0

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Grading:

The distribution of weights for the exams, homeworks and projects is as follows:

Midterm Exam 25%
Final 25%
Labs/Projects 35%
Class Participation/ Homework / Quizzes 15%

Tentative Course Outline:

(Note: Changes/Additions to this schedule will be posted on my web site http://www.cs.umbc.edu/~reza2)

Date	Topic
Week 1	Introduction to Programmable technologies (Ch. 1,2 FPGA text)
	Introduction to EDA (Ch. 1 Verilog text)
Week 2	Basics of hardware modeling (Ch. 2 Verilog text)
	Event driven simulation and test benches (Ch. 3 Verilog text), Quiz1
Week 3	FPGA architectures (Ch. 3&4 FPGA text)
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Week 4	Logic system, data types and operators in Verilog (Ch. 4 Verilog text)
	Lab: CADENCE Verilog Modeling and Simulation, Quiz 2, Project 1
Week 5	FPGA architectures (Ch. 4 FPGA text)
	Lab: ISE tutorial review

Week 6	Behavioral Description in Verilog (Ch. 7 Verilog text)
	Behavioral Description in Verilog (Ch. 7 Verilog text), Quiz 3
Week 7	Behavioral Description in Verilog (Ch. 7 Verilog text)
	Lab: Introduction to XST board, Project 2
Week 8	Midterm
	Programming an FPGA (Ch. 5 FPGA text)
Week 9	FPGA vs. ASIC Design styles (Ch. 7 FPGA text) Schematic and HDL-based design flows (Ch. 8 & 9 FPGA text)
	Lab: Finite state machines on XST board, Project 3
Week 10	Synthesis of combinational logic (Ch. 8 Verilog text)
	Lab: Introduction to Labview, Quiz 4
Week 11	Synthesis of sequential logic (Ch. 9 Verilog text)
	Lab: Introduction to Labview, Final project
Week 12	Synthesis of language constructs (Ch. 10 Verilog text)
	Lab: Final project
Week 13	Rapid prototyping with Xilinx FPGAs (Ch. 13 Verilog text)
	Lab: Final project, Quiz 5
Week 14	Design examples in Verilog (Ch. 12 Verilog text)
	Lab: Final project
Week 15	Design examples in Verilog (Ch. 12 Verilog text)
	Lab: Final project
	Final Exam

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No incompletes will be given, except as required by university policy for truly exceptional circumstances.
The final exam is cumulative. However, material covered after the second exam will be emphasized.
Students are encouraged to participate in class.
NOTE: Cheating at any time in this course will cause you to fail the course. Please refer to the following guidelines.
For a complete description of academic dishonesty, refer to the UMBC Student Handbook.

The following is taken from the UMBC Student Handbook:
DEFINITIONS OF ACADEMIC MISCONDUCT
Academic misconduct may include but is not limited to the following:
Cheating: knowingly using or attempting to use unauthorized material, information, or study aids in any academic exercise. Fabrication: Intentional and unauthorized falsification or invention of any information or citation in an academic exercise.
Facilitating Academic Dishonesty: Intentionally or knowingly helping or attempting to help another commit an act of academic dishonesty.
Plagiarism: Knowingly representing the words or ideas of another as one's own in any academic exercise, including works of art and computer-generated information/ images.
POLICY FOR RESOLVING CASES OF ACADEMIC MISCONDUCT
Individual faculty members have the right and responsibility to deal directly with any cases of academic misconduct which arise in their courses. Instances of academic misconduct may be identified in one of two ways. If a faculty member believes a student has committed an act of academic misconduct--for example, by direct observation of student behavior, by comparing the contents of an assignment with that submitted by another student, or by reviewing notated sources or references--the faculty member, in consultation with the Chair of the Academic Conduct Committee, will assess the student's alleged misconduct and the faculty member's options. If a student believes that academic misconduct has occurred, the student will notify either the faculty member or the Chair of the Academic Conduct Committee.
It is particularly important that the Chair of the Academic Conduct Committee be consulted. The Chair can provide knowledge and insight for the faculty member. Communication of instances of academic misconduct also protects the integrity of the university by providing a means of recording infractions that may be repeated by a particular student, or which may prove endemic to a particular course or department.
Consultation with the Chair of the Academic Conduct Committee provides a formal record of the infraction and resolution, protecting the student, professor, and university should any questions later arise. The student will have the opportunity to respond to an accusation of academic misconduct.