Event Driven Simulation and Test-benches

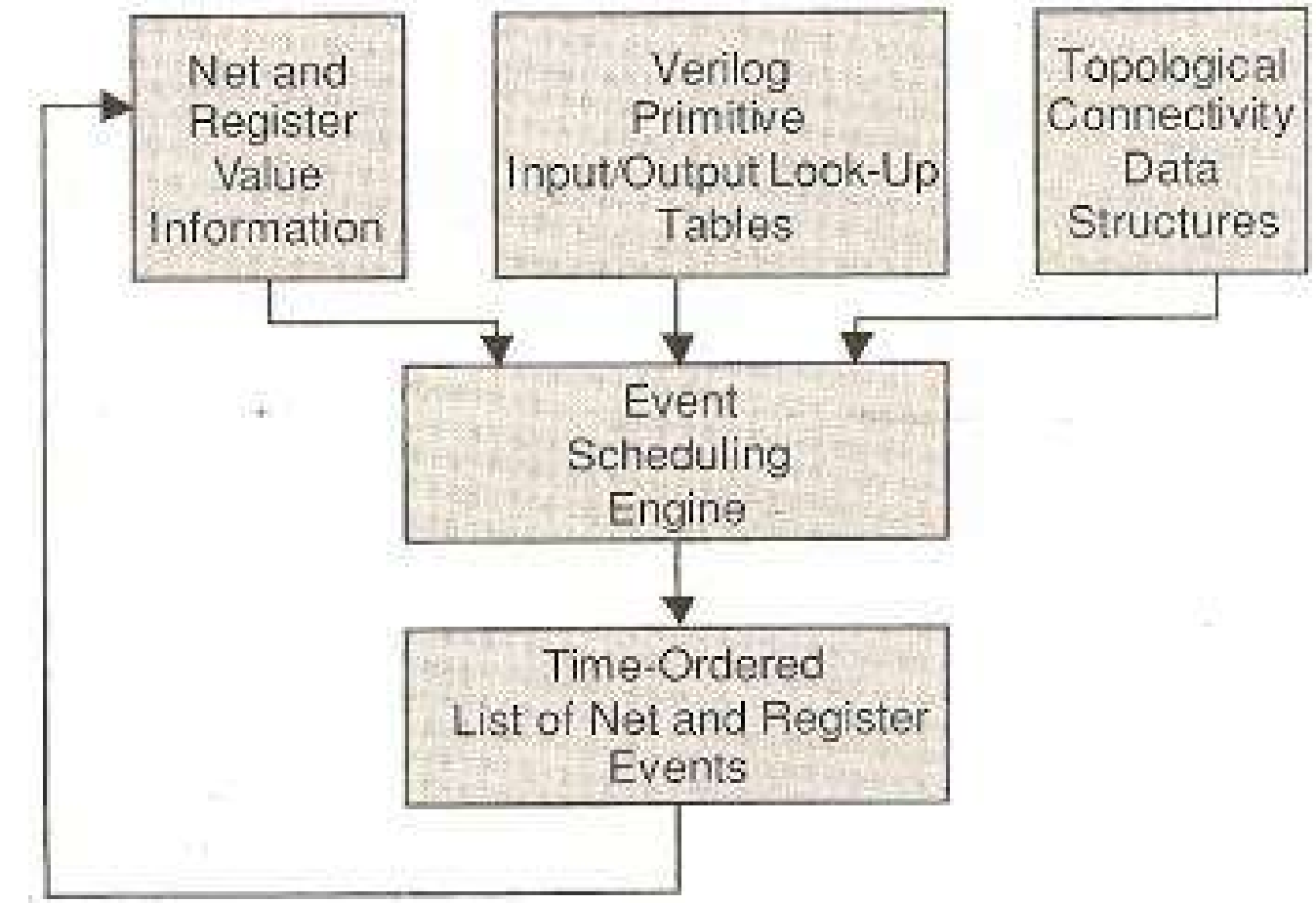
Event Driven Simulation

- Continuous time and value simulation used for analog circuits
- Differential equations should be solved
- Very slow, too much accuracy for digital circuits

Event Driven Simulation

- Discrete values used for digital circuits
- ‘1’,’0’,’Z’ and ‘X’ used in verilog
- This reduces the complexity of simulation
- In digital circuits event driven approach is used instead of continuous time simulation
- This also reduces complexity of simulation

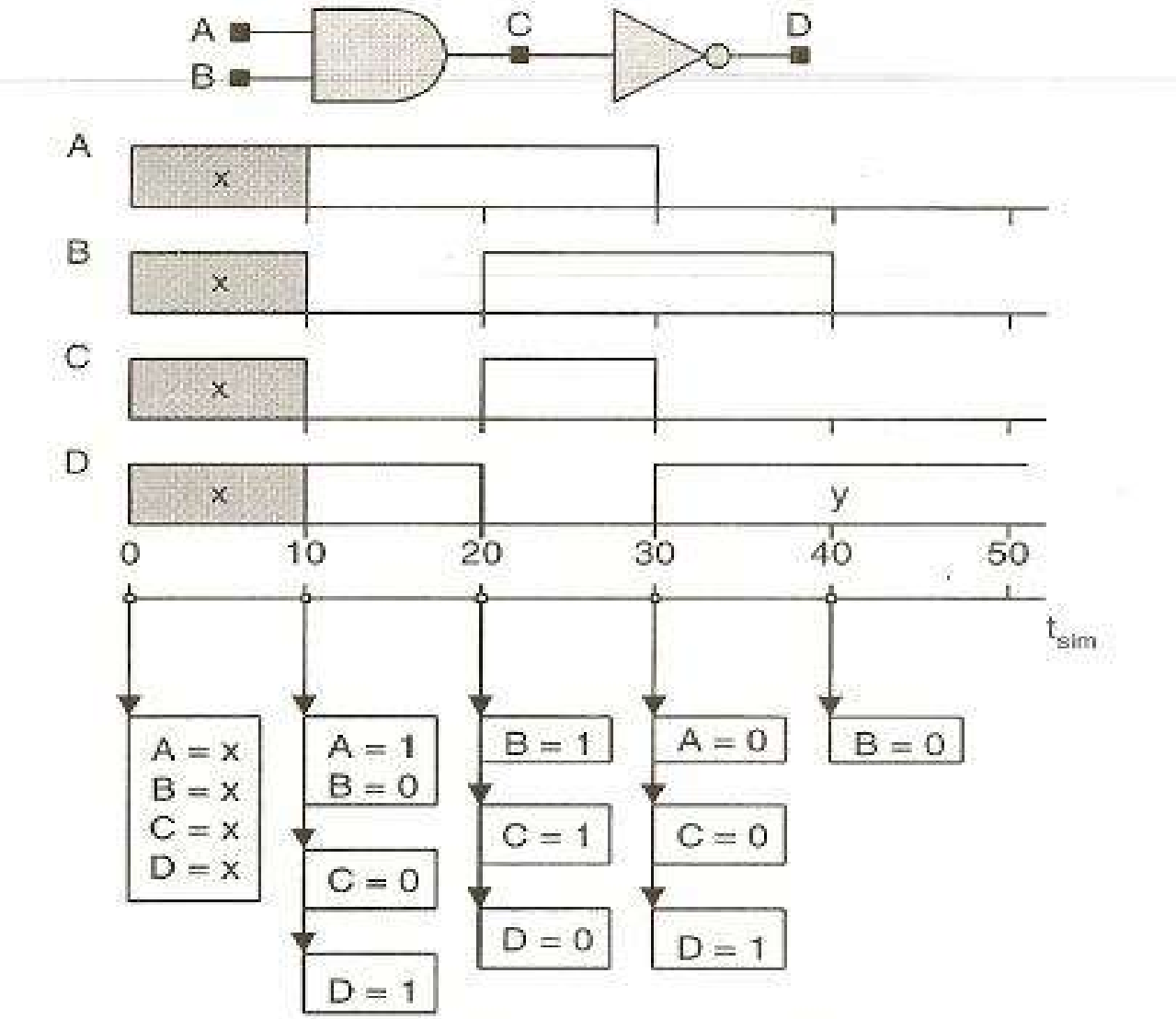
Event Driven Simulation



Organization of an event-driven simulator.

Example

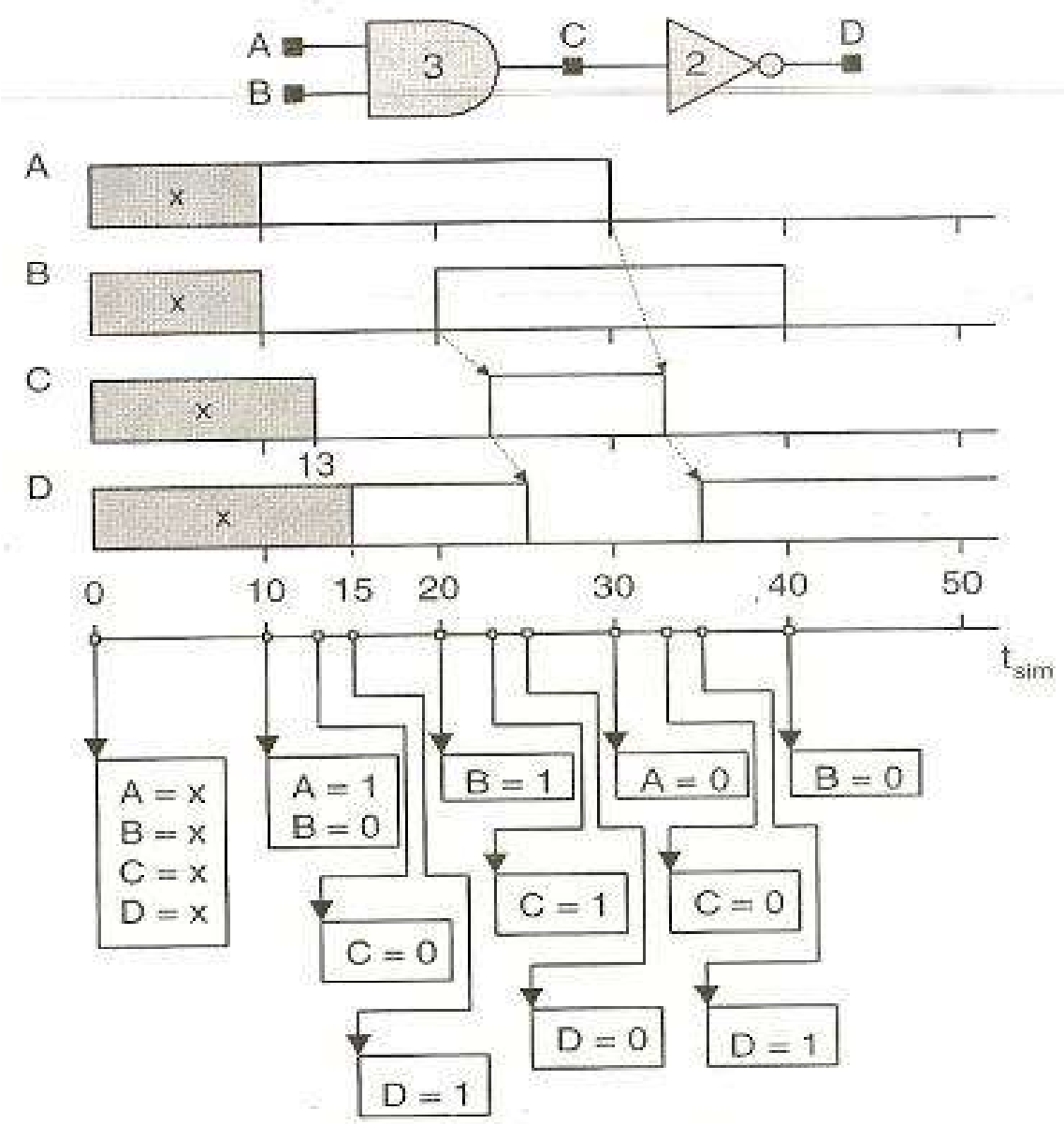
- Zero-delay



Representation of data structures for event-driven simulation.

Example

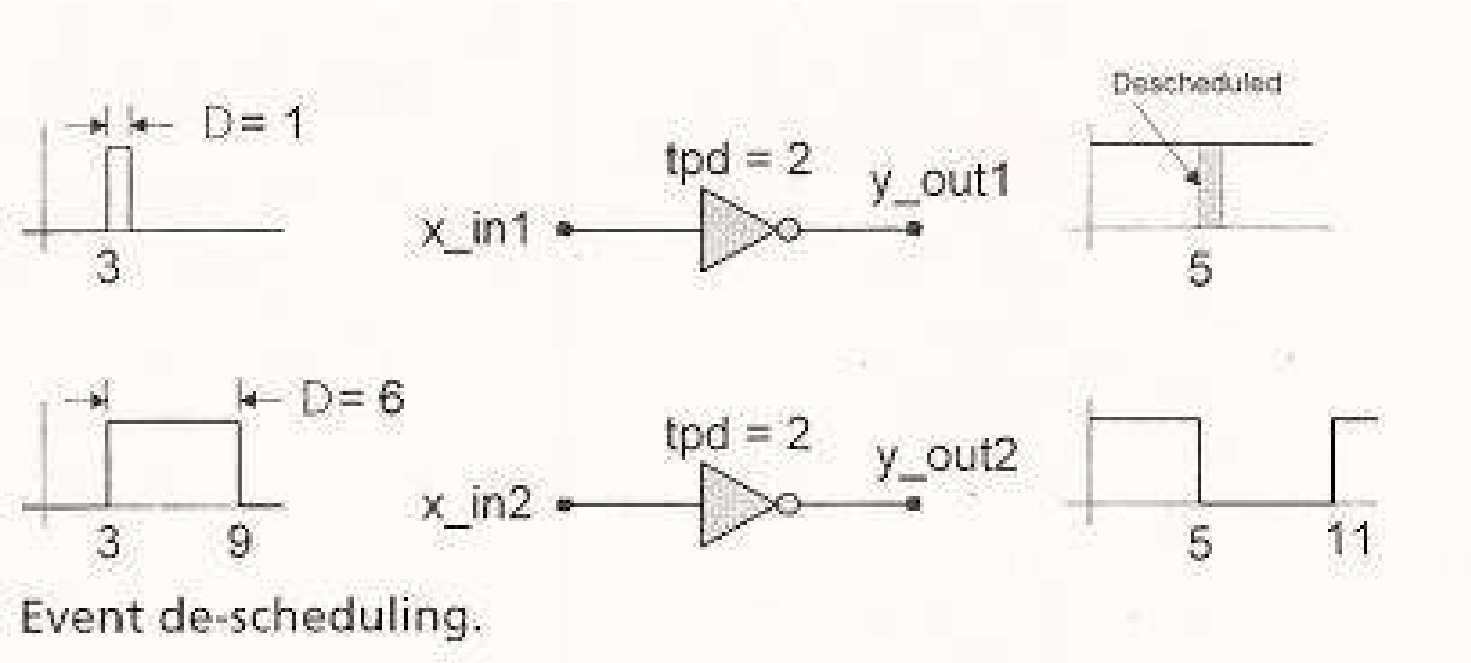
- Effect of delay



Data structures and event propagation delay.

The idea of Inertial Delay

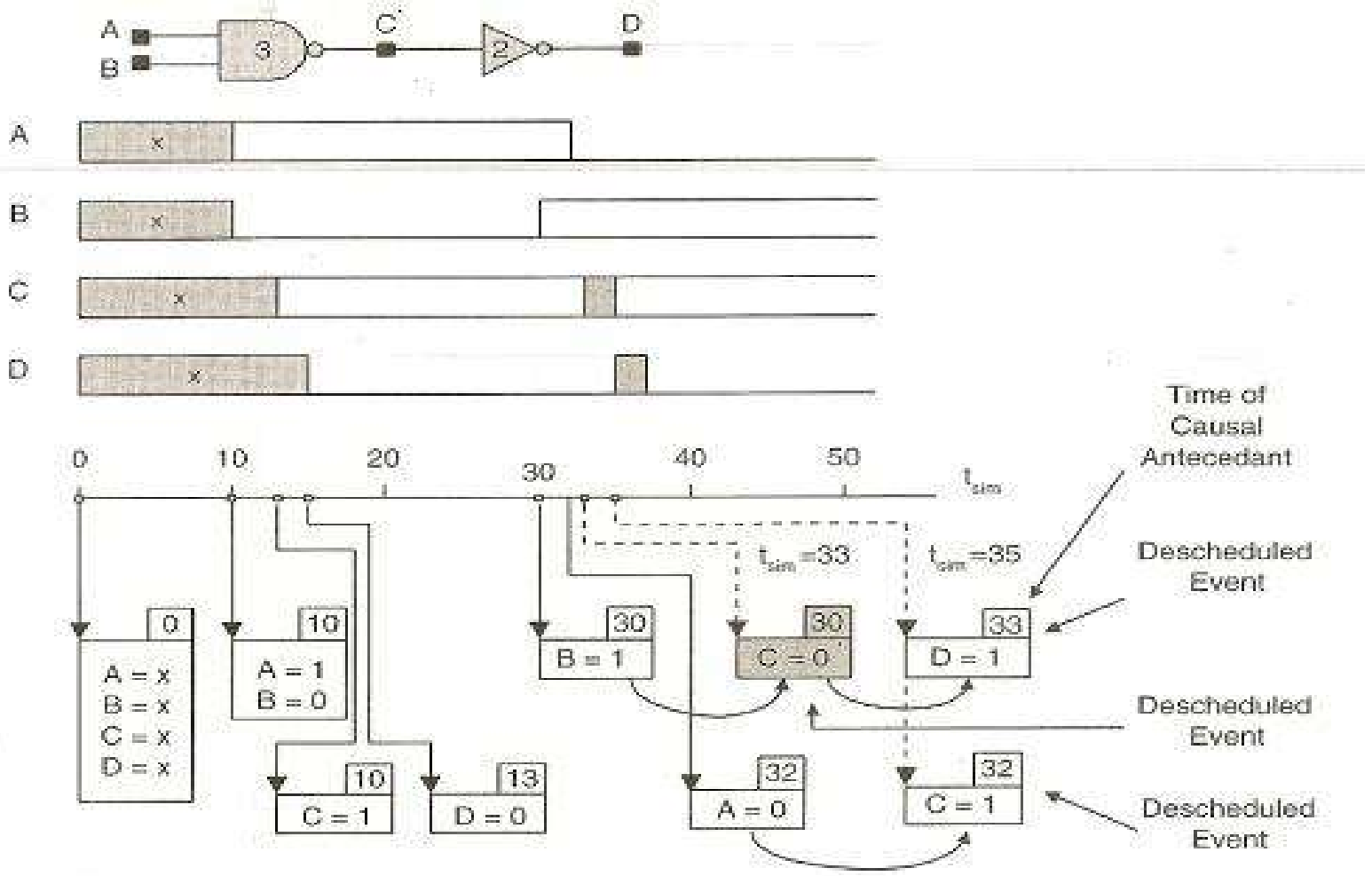
- To model time required for charge transitions
- Close to what happens in RC circuits



Event de-scheduling.

Inertial Delay

- Verilog simulators work based on inertial delay model, event De-scheduling is required



Example of event de-scheduling.

Test-Benches

- Example

```
module test_Nand_Latch_1;                          // Design Unit Testb
   reg      preset, clear;
   wire     q, qbar;

   Nand_Latch_1 M1 (q, qbar, preset, clear);       // Instantiate UUT

   initial                                         // Create DUTB response monitor
      begin
         $monitor ($time, "preset = %b clear = %b q = %b
                           qbar = %b", preset, clear, q, qbar);
      end

   initial
      begin                                        // Create DUTB stimulus generator
         #10    preset    = 0;    clear = 1;
         #10    preset    = 1;    $stop;     // Enter. to proceed
         #10    clear     = 0;
         #10    clear     = 1;
         #10    preset    = 0;
      end

   initial
      #60    $finish ;                 // Stop watch
endmodule
```