Basic I/O Instructions

IN and ***OUT*** transfer data between an I/O device and the microprocessor's accumulator (AL, AX or EAX).

The I/O address is stored in:

- Register DX as a 16-bit I/O address (variable addressing).
- The byte, p8, immediately following the opcode (fixed address).

```
IN   AL, 19H    ;8-bits are saved to AL from I/O port 19H.
IN   EAX, DX    ;32-bits are saved to EAX.
OUT  DX, EAX    ;32-bits are written to port DX from EAX.
OUT  19H,AX     ;16-bits are written to I/O port 0019H.
```

Only 16-bits (A_0 to A_{15}) are decoded.

Address connections above A_{15} are undefined for I/O instructions.

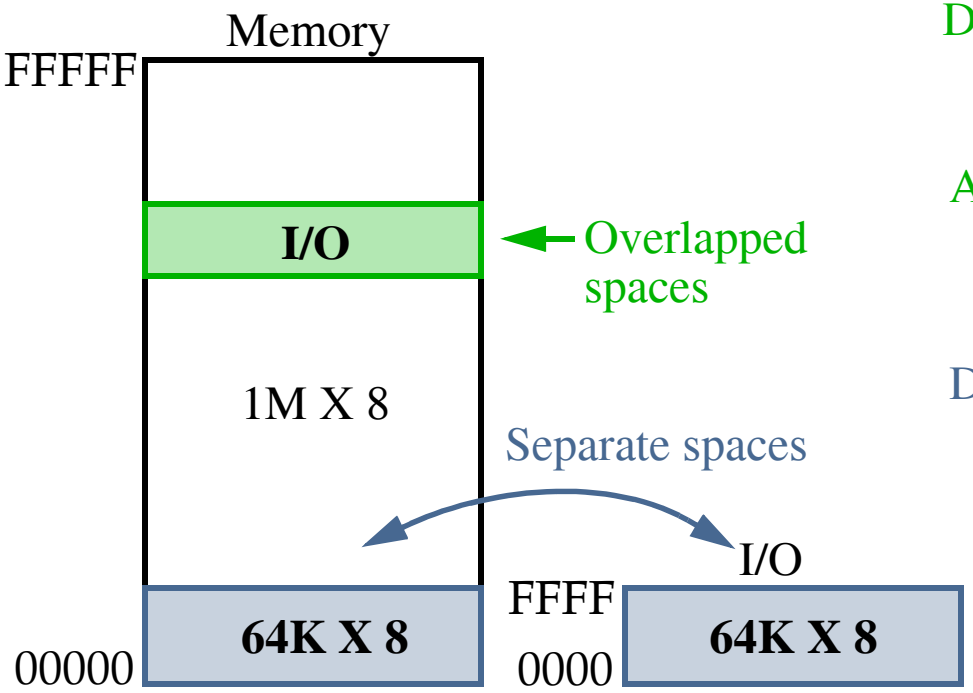
0000H-03XXH are used for the ISA bus.

INS and OUTS transfer to I/O devices using ES:DI and DS:SI, respectively.

Isolated versus Memory-Mapped I/O

Isolated and Memory-Mapped I/O

- In the Isolated scheme, IN, OUT, INS and OUTS are required.
- In the Memory-mapped scheme, any instruction that references memory can be used
- .



Disadvantage:
A portion of the memory space is used for I/O devices.

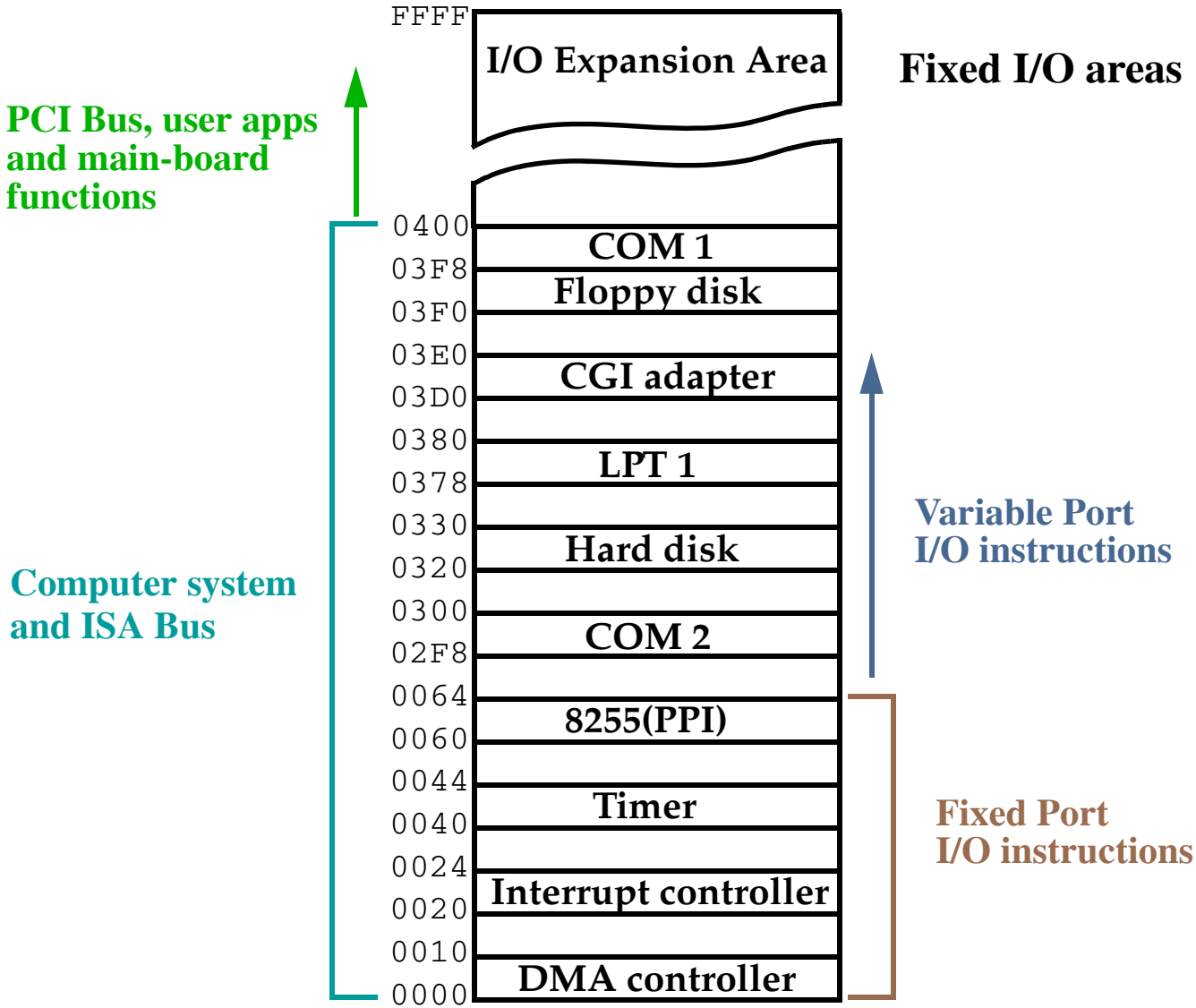
Advantage:
$\overline{IORC}$ and $\overline{IOWC}$ not required.
Any data transfer instruction.

Disadvantage:
Hardware using M/$\overline{IO}$ and W/$\overline{R}$ needed to develop signals $\overline{IORC}$ and $\overline{IOWC}$.
Requires IN, OUT, INS and OUTS

8-bit port addresses used to access system board device, e.g. timer and keyboard.

16-bit port addresses used to access serial and parallel ports, harddrives, etc.

I/O Map

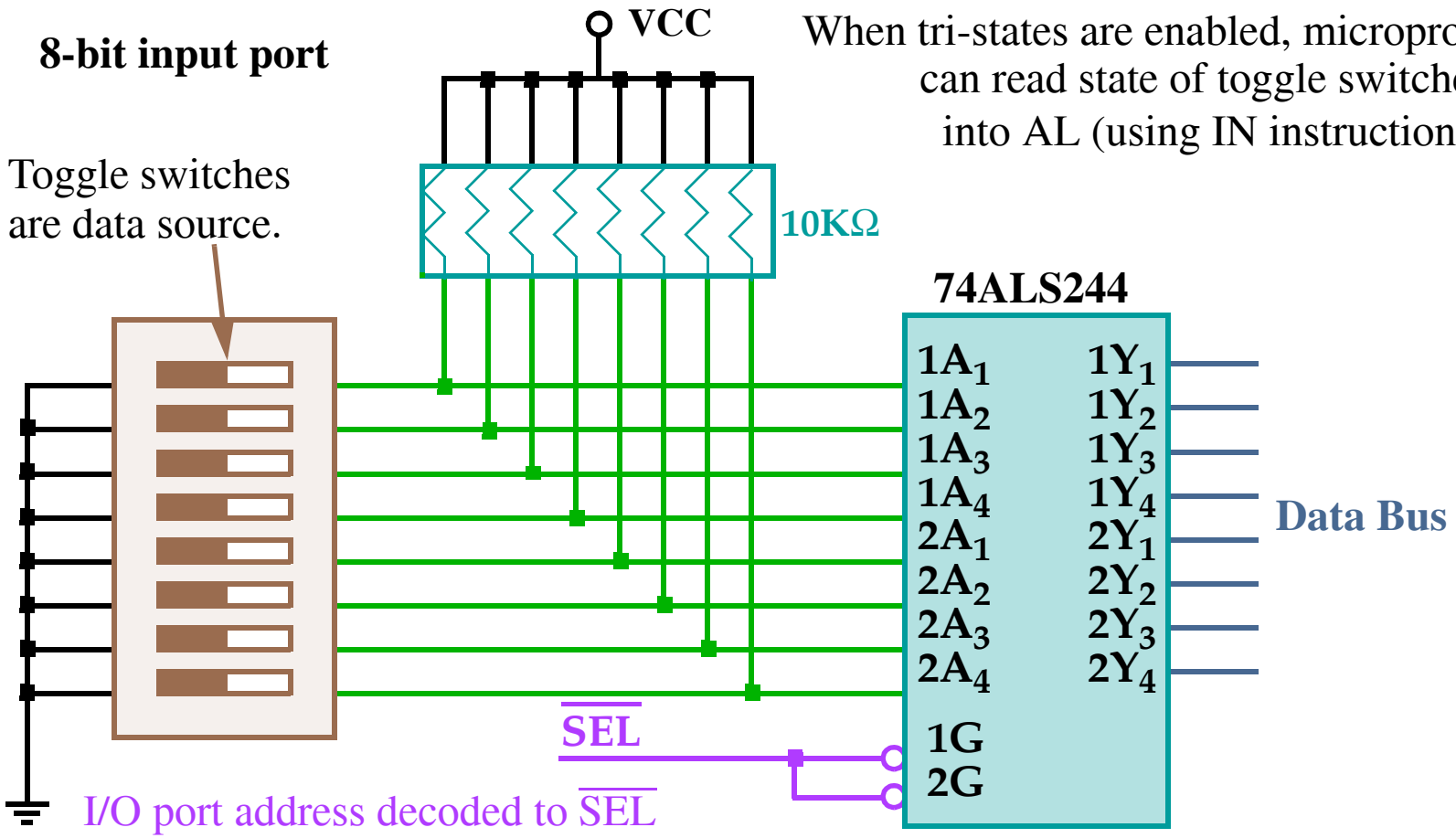

FFFF
I/O Expansion Area
Fixed I/O areas
PCI Bus, user apps and main-board functions
0400
COM 1
03F8
Floppy disk
03F0
03E0
CGI adapter
03D0
0380
LPT 1
0378
0330
Hard disk
0320
Computer system and ISA Bus
0300
COM 2
02F8
0064
8255(PPI)
0060
0044
Timer
0040
0024
Interrupt controller
0020
0010
DMA controller
0000
Variable Port I/O instructions
Fixed Port I/O instructions

Basic I/O Interface

The basic input device (to the microprocessor) is a set of tri-state buffers.

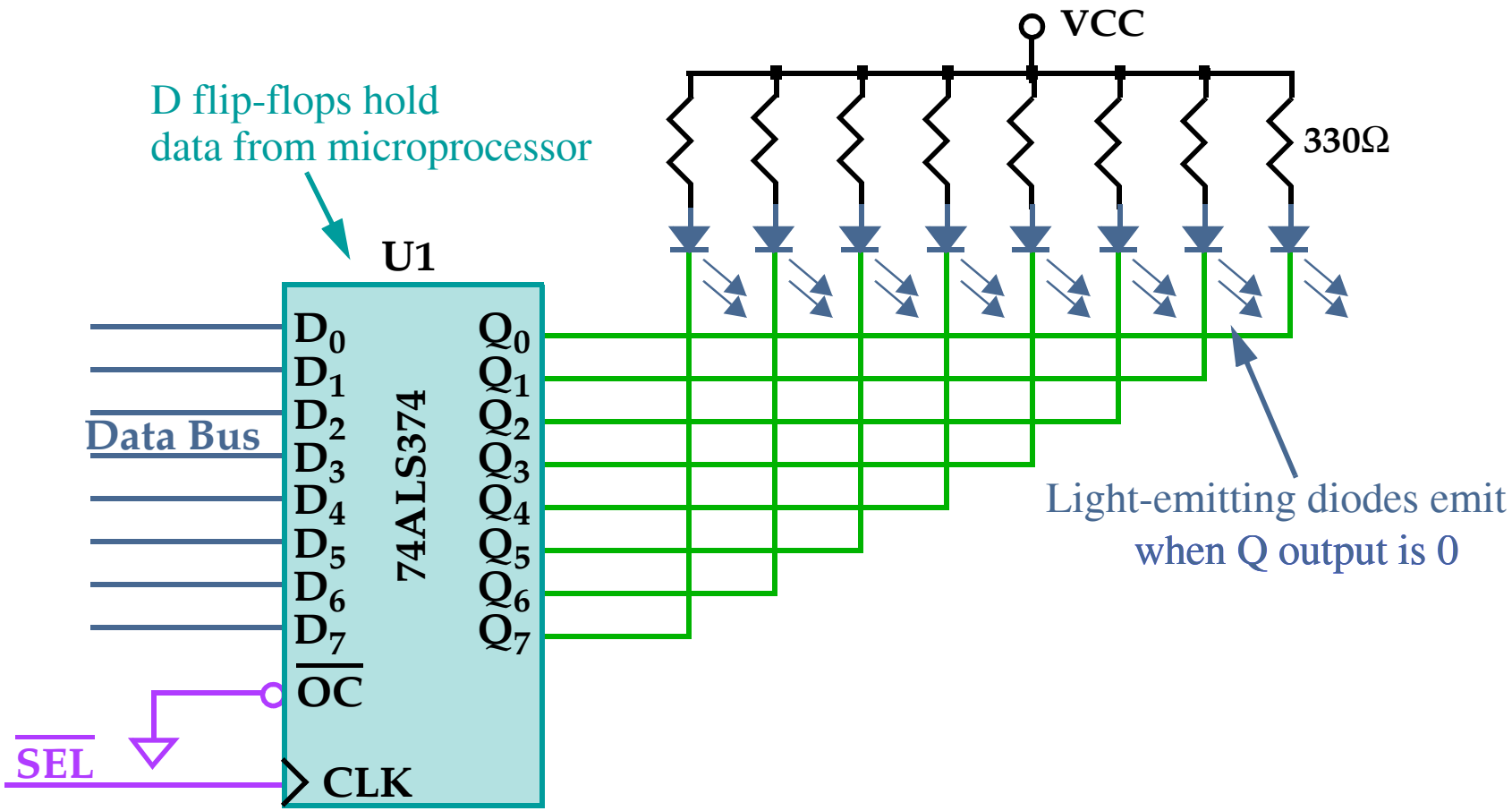
The basic output device (from the microprocessor) is a set of latches.

Basic Input Interface:



Basic I/O Interface

Basic Output Interface:



In this case, the data from the OUT instruction is latched using $\overline{\text{SEL}}$.

Handshaking

I/O devices are typically slower than the microprocessor.

Handshaking is used to synchronize I/O with the microprocessor.

A device indicates that it is ready for a command or data (through some I/O pin or port).

The processor issues a command to the device, and the device indicates it is busy (not ready).

The I/O device finishes its task and indicates a ready condition, and the cycle continues.

There are two basic mechanisms for the processor to service a device.

- ***Polling: Processor initiated***. Device indicates it is ready by setting some status bit and the processor periodically checks it.
- ***Interrupts: Device initiated***. The act of setting a status bit causes an interrupt, and the processor calls an ISR to service the device.

Interfacing Circuitry

The terminal characteristics of the processor must be matched to those of the I/O devices.

Input Devices:

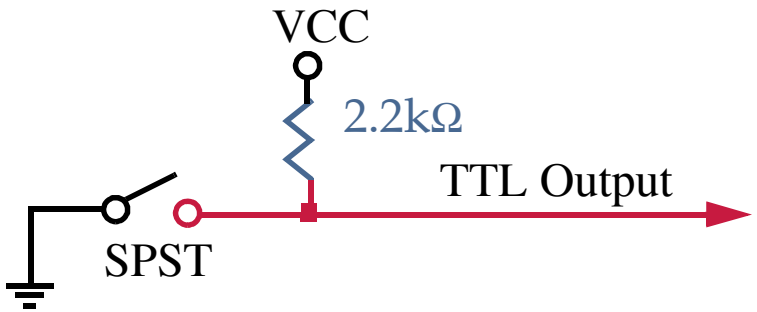
They are either:

- TTL (0.0V-0.8V low and 2.0-5.0V high) or compatible.
- Switch-based; usually either open or connected.

These must be conditioned before they can be used properly.

For example, to make a simple (single-pole, single-throw) toggle switch TTL compatible:

This ensures that the output is held at either 0 or logic 1 at all times (it never floats).



The value of R can vary between 1K and 10KΩ.

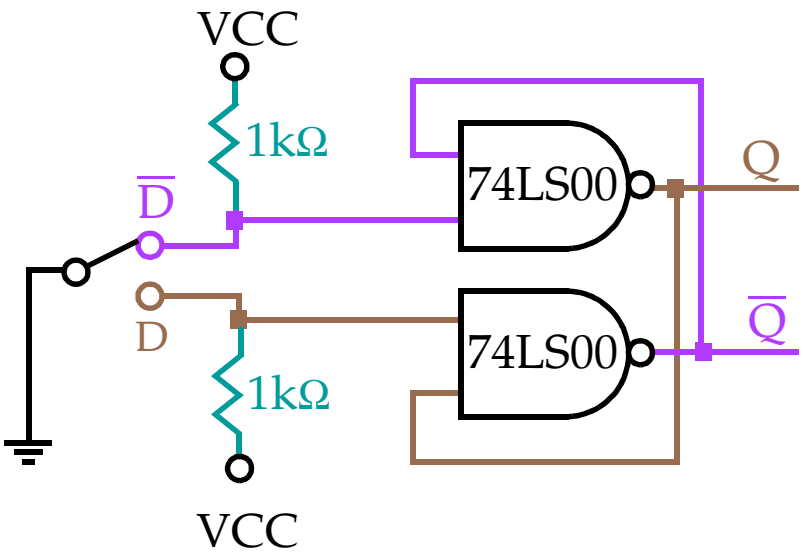
Interfacing Circuitry

Input Devices:

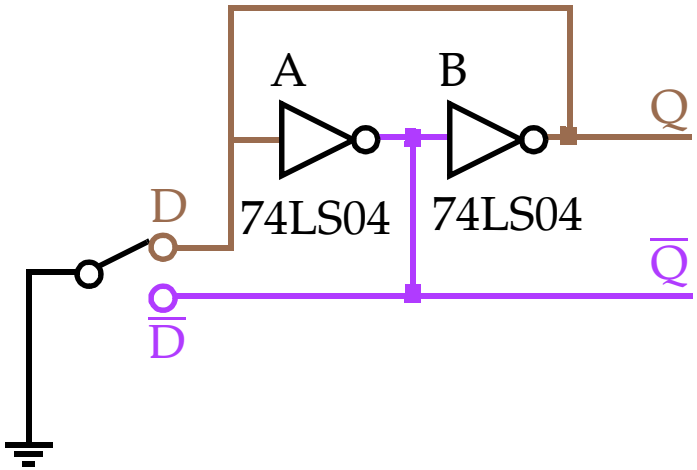
Mechanical switches physically bounce when they are closed (causing them to momentarily open after being closed).

This can cause a problem if they are used as a clocking signal.

Two asynchronous flip-flop solutions are given below:



Cross-coupled NANDs.



More practical inverter implementation

The basic idea is that these flip-flops store the values even if the D/$\overline{D}$ nodes both float.

Interfacing Circuitry

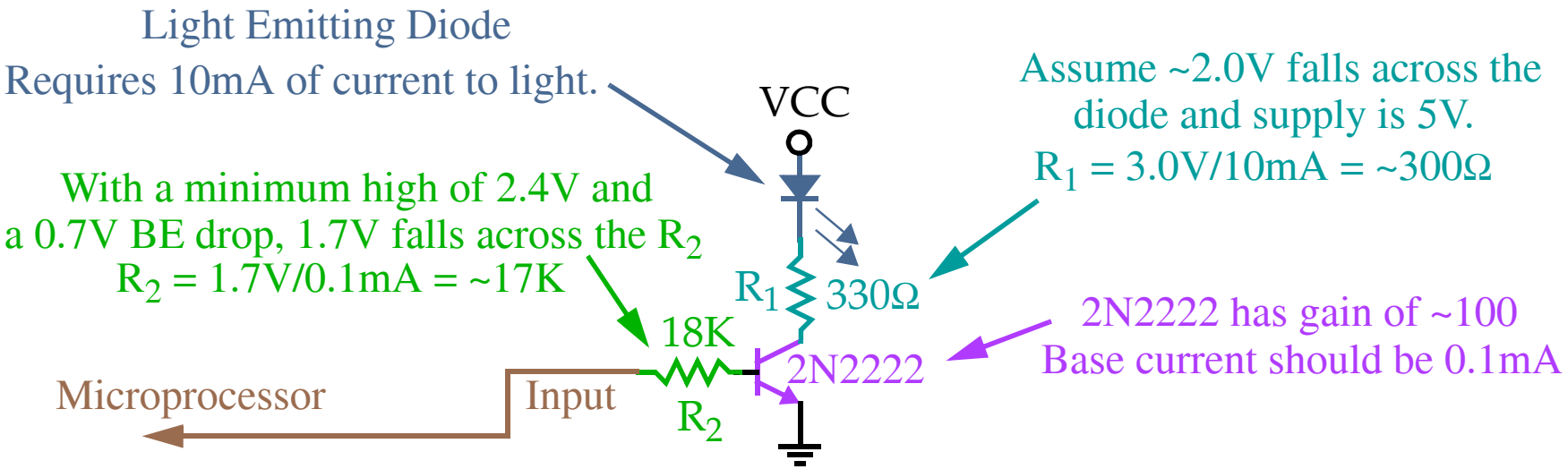
Output Devices:

Interfacing an output device requires matching the voltage and current relationships of the devices and processor.

Remember that the standard output levels of TTL compatible devices are 0.0 to 0.4V for logic 0 and 2.4V to 5.0V for logic 1.

The current levels are 0.0 to 2.0mA (logic 0) and 0.0 to -400uA (logic 1).

For example:



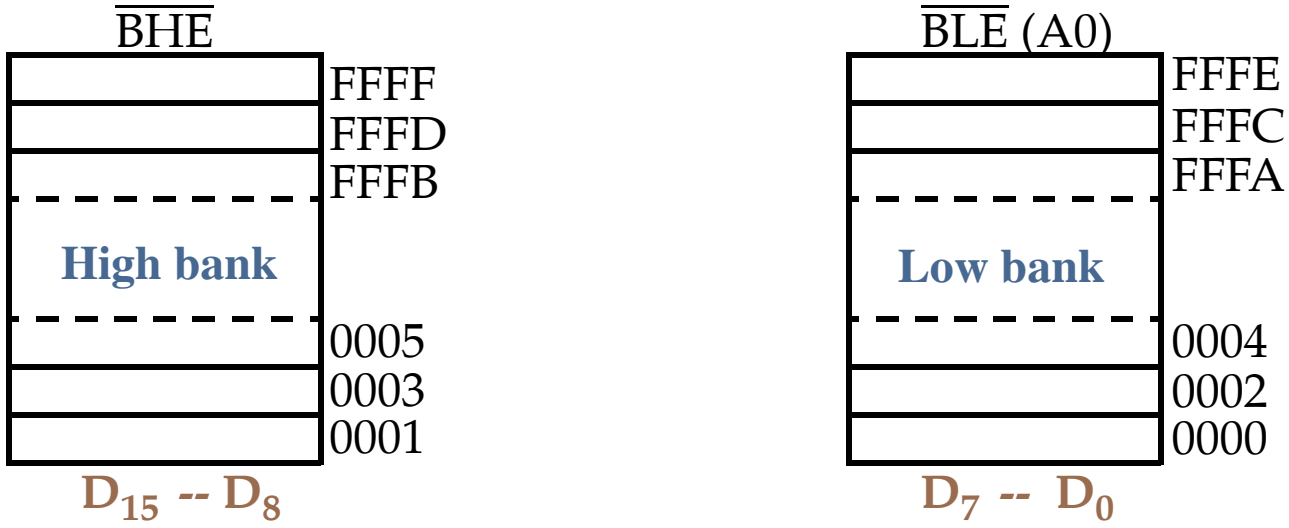
I/O Port Decoding

For memory-mapped I/O, decoding is identical to memory decoding.

For isolated I/O, $\overline{\text{IORC}}$ and $\overline{\text{IOWC}}$ are developed using M/$\overline{\text{IO}}$ and W/$\overline{\text{R}}$ pins of the micro-processor.

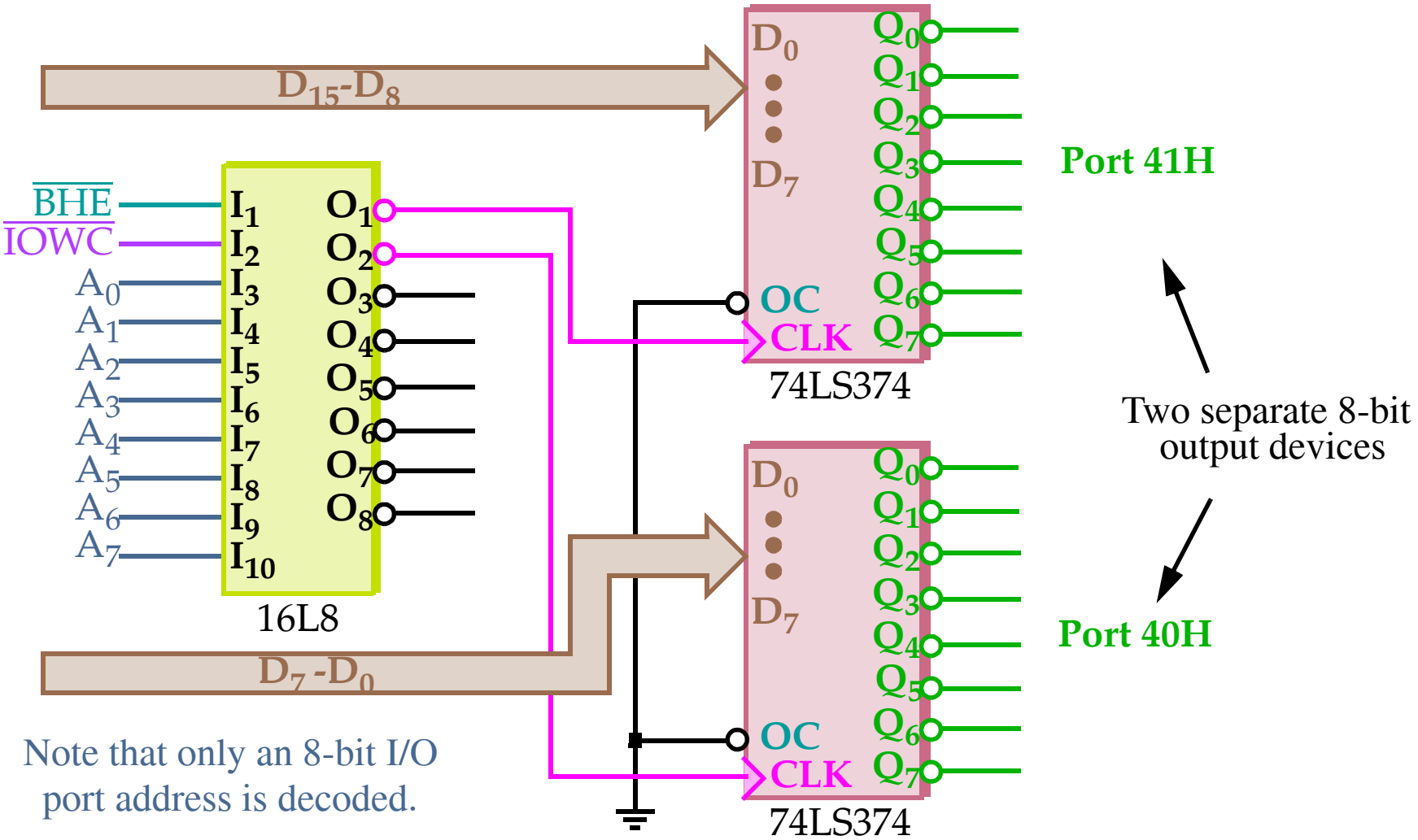
The text gives examples of 8-bit decoding and 16-bit decoding, which is a straightforward application of devices we've used for memory decoding.

The I/O banks on the 8086 through the 80386SX are also set up like the memory.



I/O Port Decoding

Similar to memory writes, any 8-bit I/O write request requires separate write strobes ($\overline{BHE}$ and $\overline{BLE}$) but read requests do not.



I/O Port Decoding

Output devices can be 16-bit in which case $\overline{\text{BHE}}$ is not needed.

Input devices can be 8-bit or 16-bit.

Note that instead of latches, high impedance buffers (74ALS244) are used in these cases.

32-bit ports are becoming more popular because of PCI bus primarily.

The EISA and VESA local bus are also 32-bit buses.

For the 64-bit data buses of the Pentium, the I/O ports can appear in any of the 8 banks.

However, only 32-bit transfers are supported, as there are no 64-bit transfer instructions.

Programmable Peripheral Interface (82C55)

The 82C55 is a popular interfacing component, that can interface any TTL-compatible I/O device to the microprocessor.

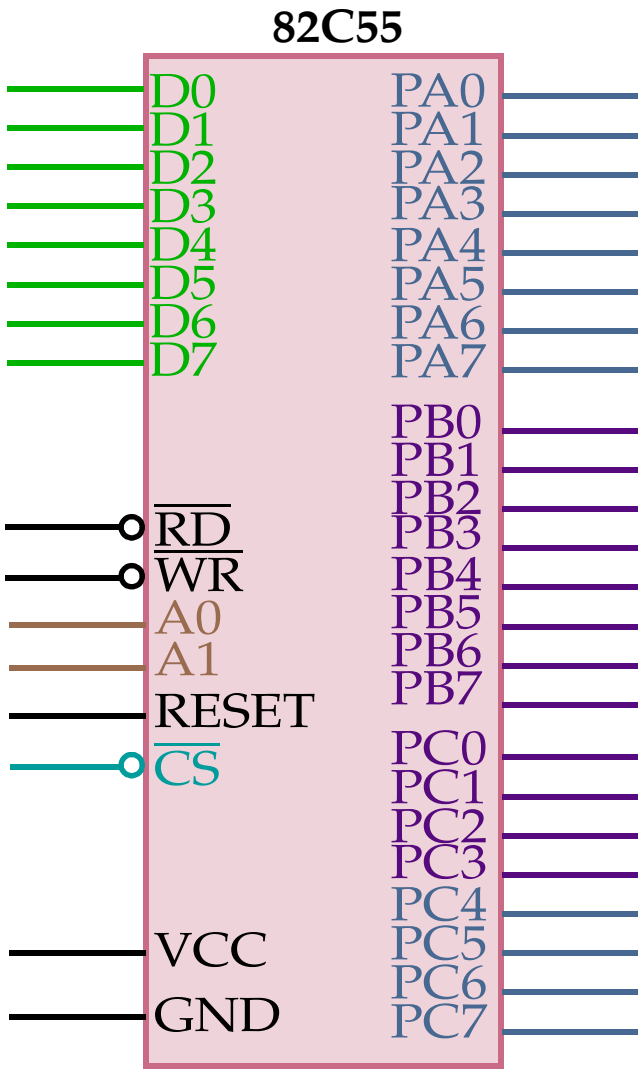
It is used to interface to the keyboard and a parallel printer port in PCs (usually as part of an integrated chipset).

Requires insertion of wait states if used with a microprocessor using higher that an 8 MHz clock.

PPI has 24 pins for I/O that are programmable in groups of 12 pins and has three distinct modes of operation.

In the PC, an 82C55 or its equivalent is decoded at I/O ports 60H-63H.

Pinout of 82C55 PPI



Group A

Port A (PA7-PA0) and upper half of port C (PC7 - PC4)

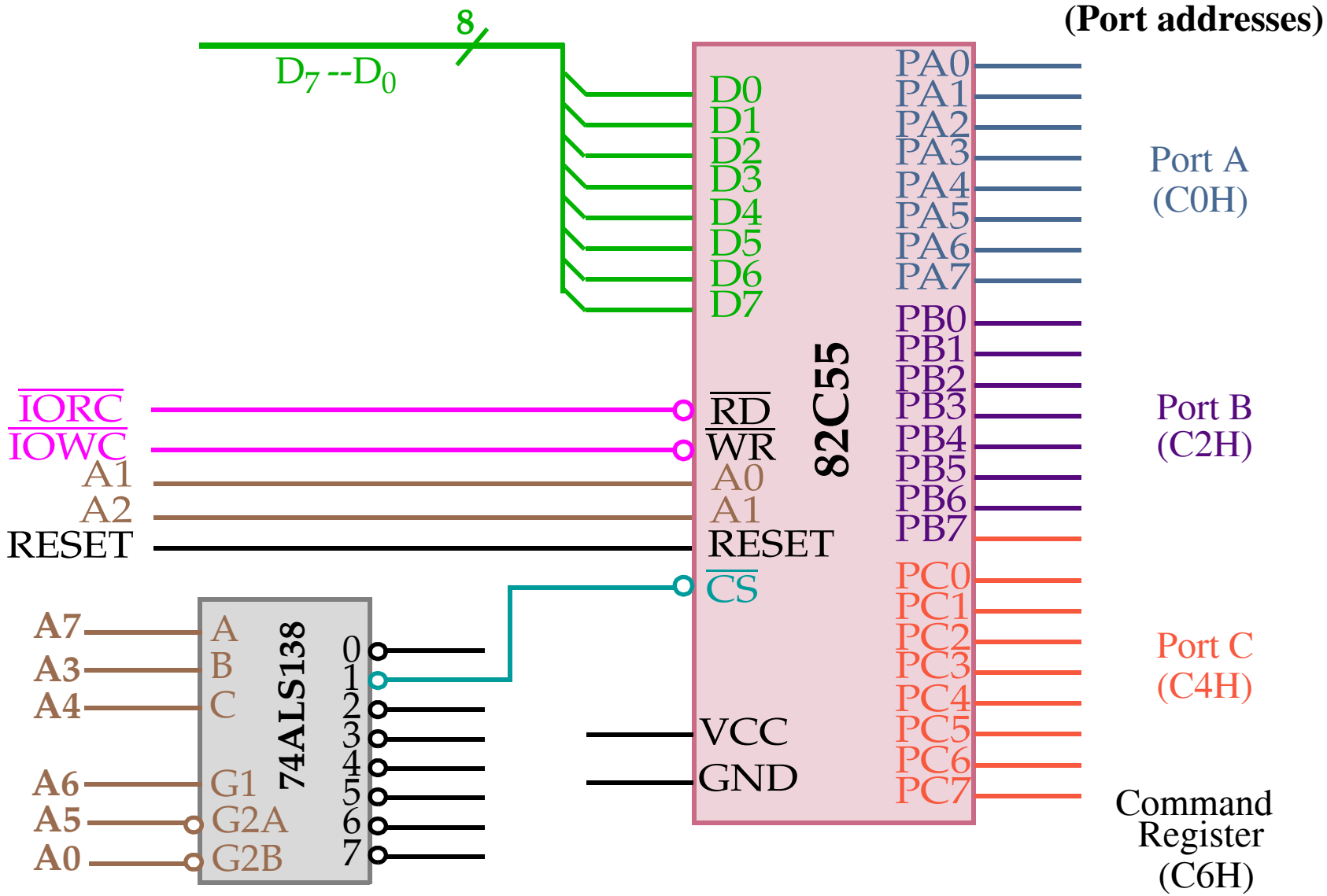
Group B

Port B (PB7-PB0) and lower half of port C (PC3 - PC0)

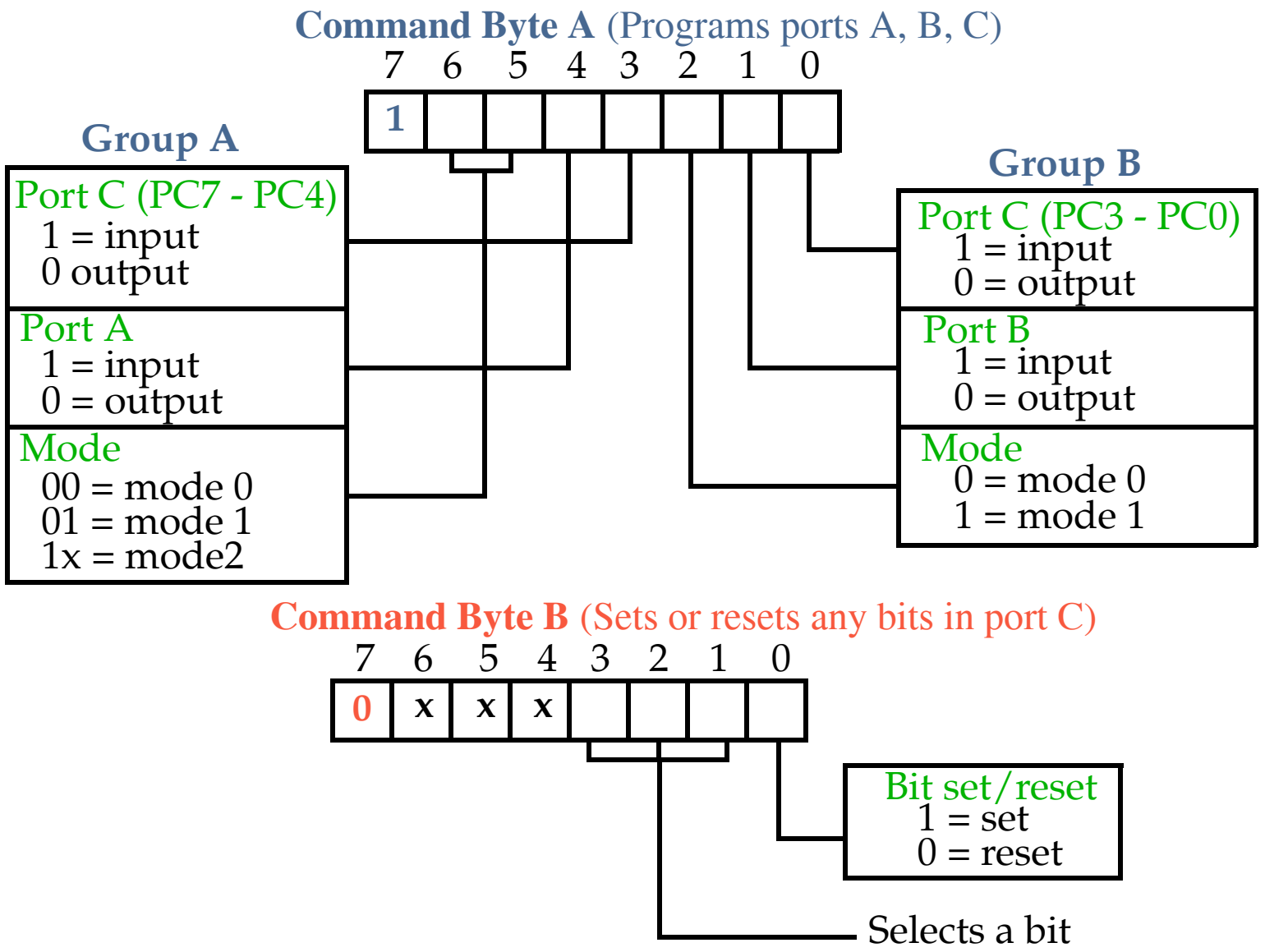
I/O Port Assignments

A_1	A_0	*Function*
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Command Register

Interfacing the 82C55 PPI

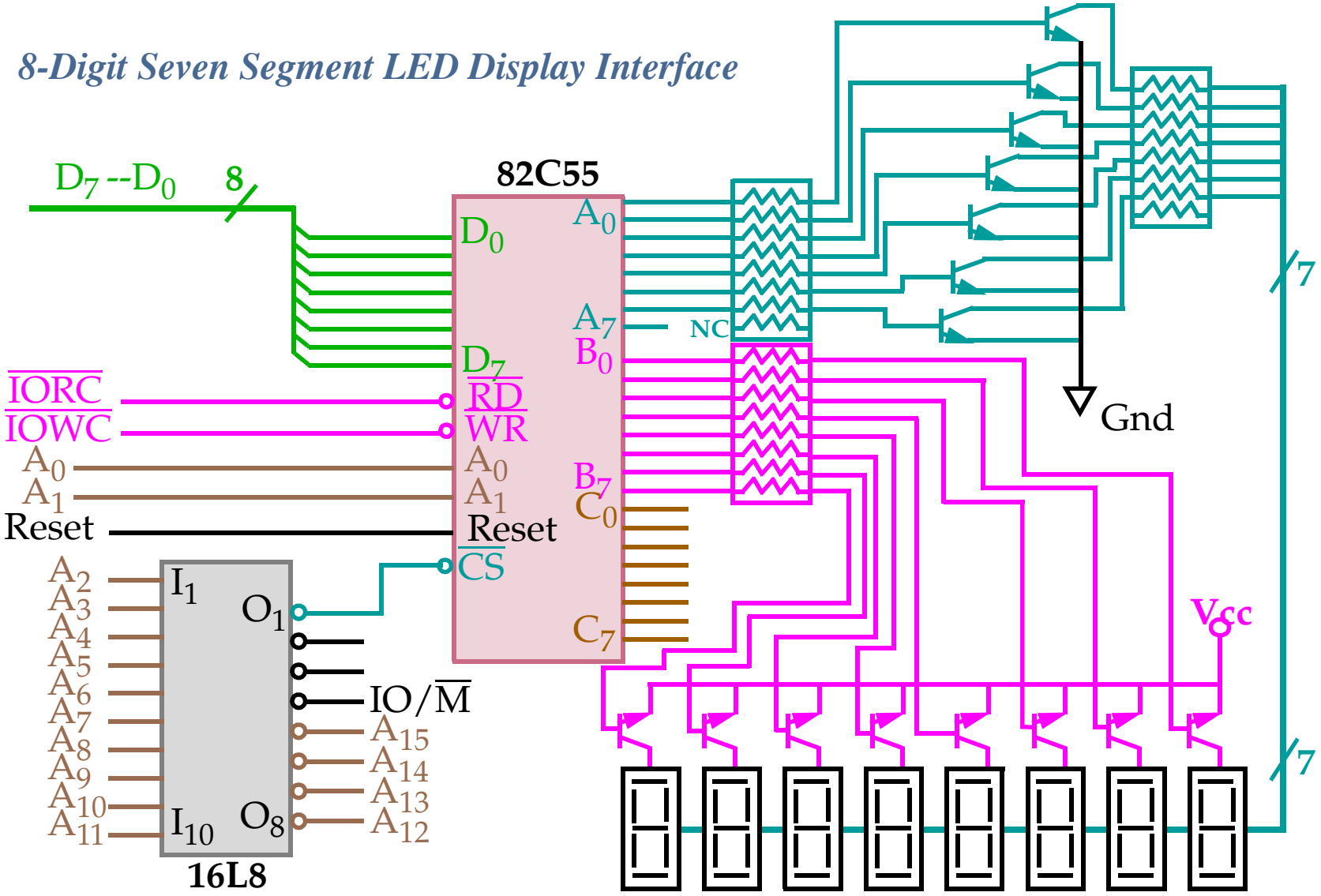


Programming the 82C55



82C55: Mode 0 Operation

8-Digit Seven Segment LED Display Interface



82C55: Mode 0 Operation

Mode 0 operation causes the 82C55 to function as a buffered input device or as a latched output device.

In previous example, both ports A and B are programmed as (mode 0) simple latched output ports.

Port A provides the segment data inputs to display and port B provides a means of selecting one display position at a time.

Different values are displayed in each digit via fast time multiplexing.

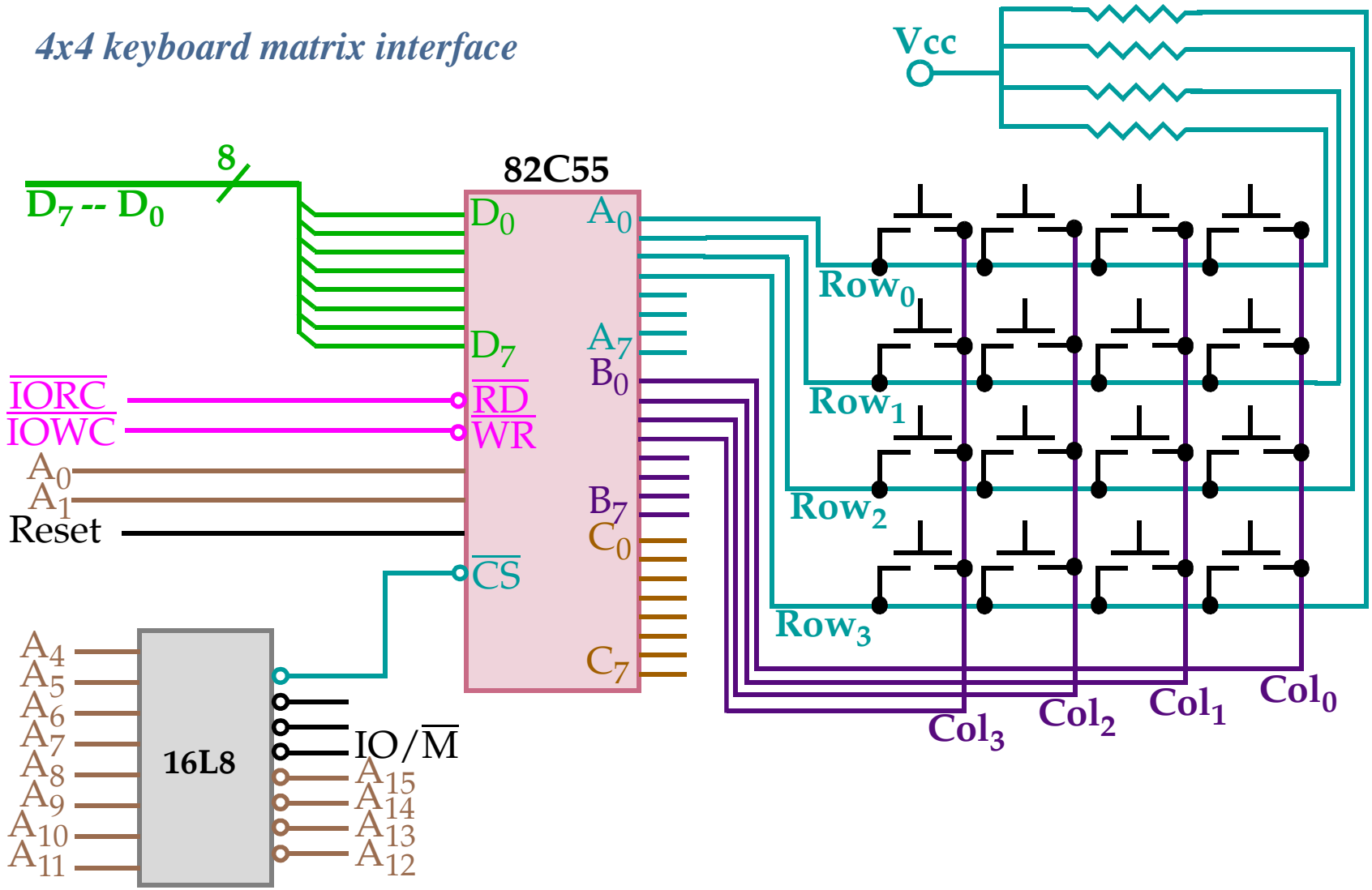
The values for the resistors and the type of transistors used are determined using the current requirements (see text for details).

Textbook has the assembly code fragment demonstrating its use.

Examples of connecting LCD displays and stepper motors are also given.

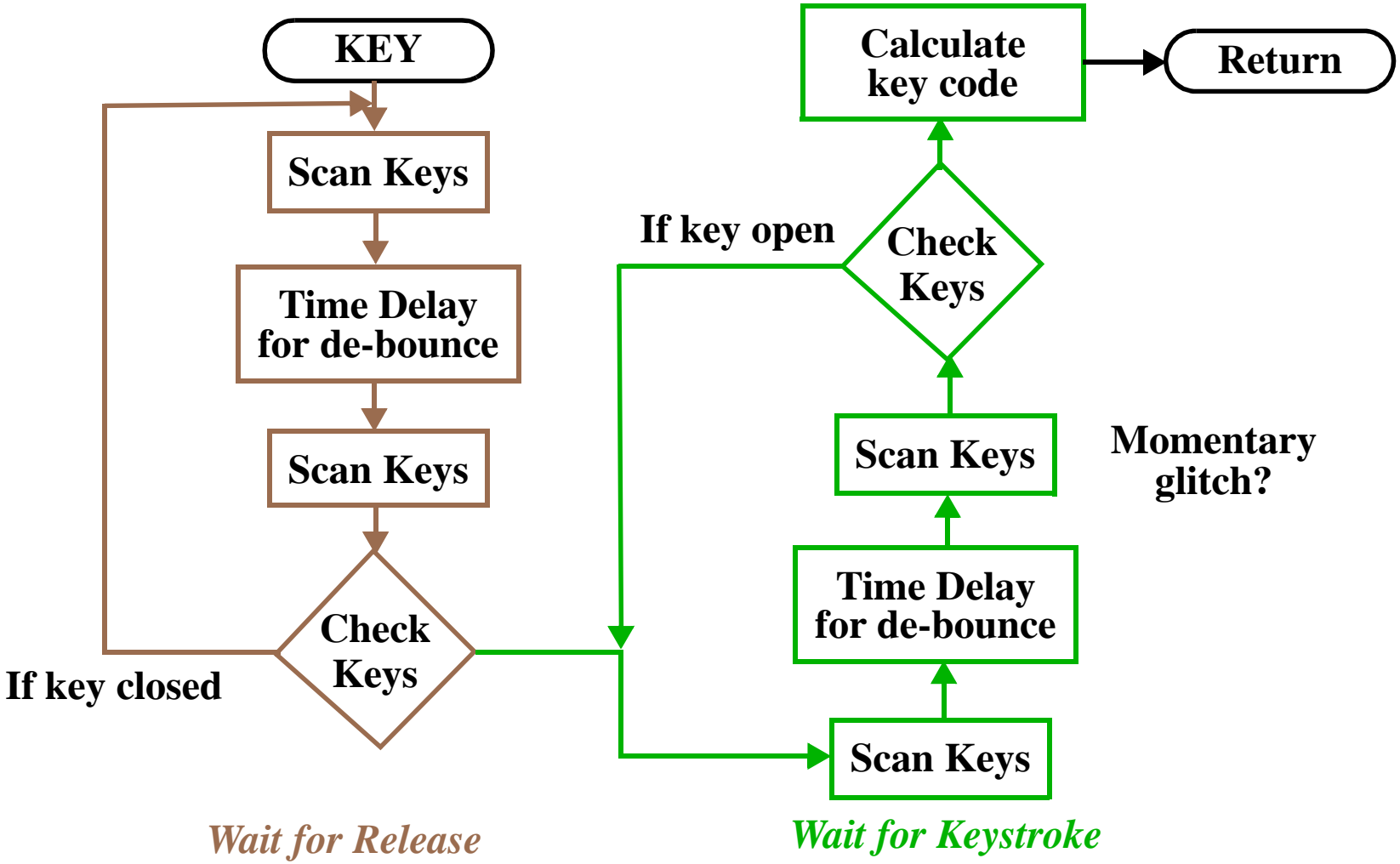
82C55: Mode 0 Operation

4x4 keyboard matrix interface



82C55: Mode 0 Operation

Flow chart of a keyboard-scanning procedure



82C55: Mode 1 Strobed Input

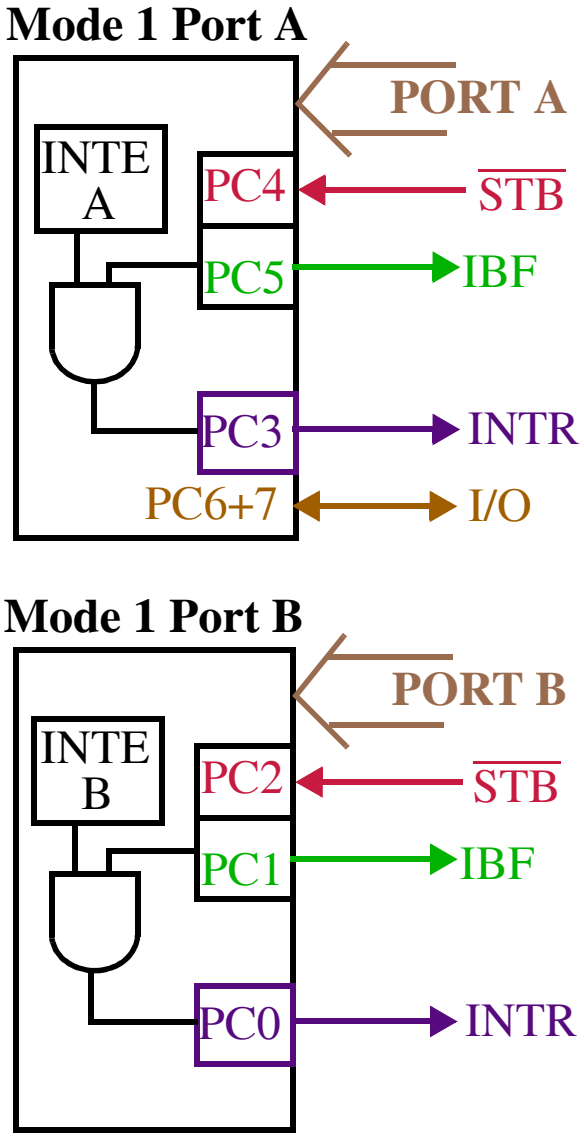
Port A and/or port B function as latching input devices. External data is stored in the ports until the microprocessor is ready.

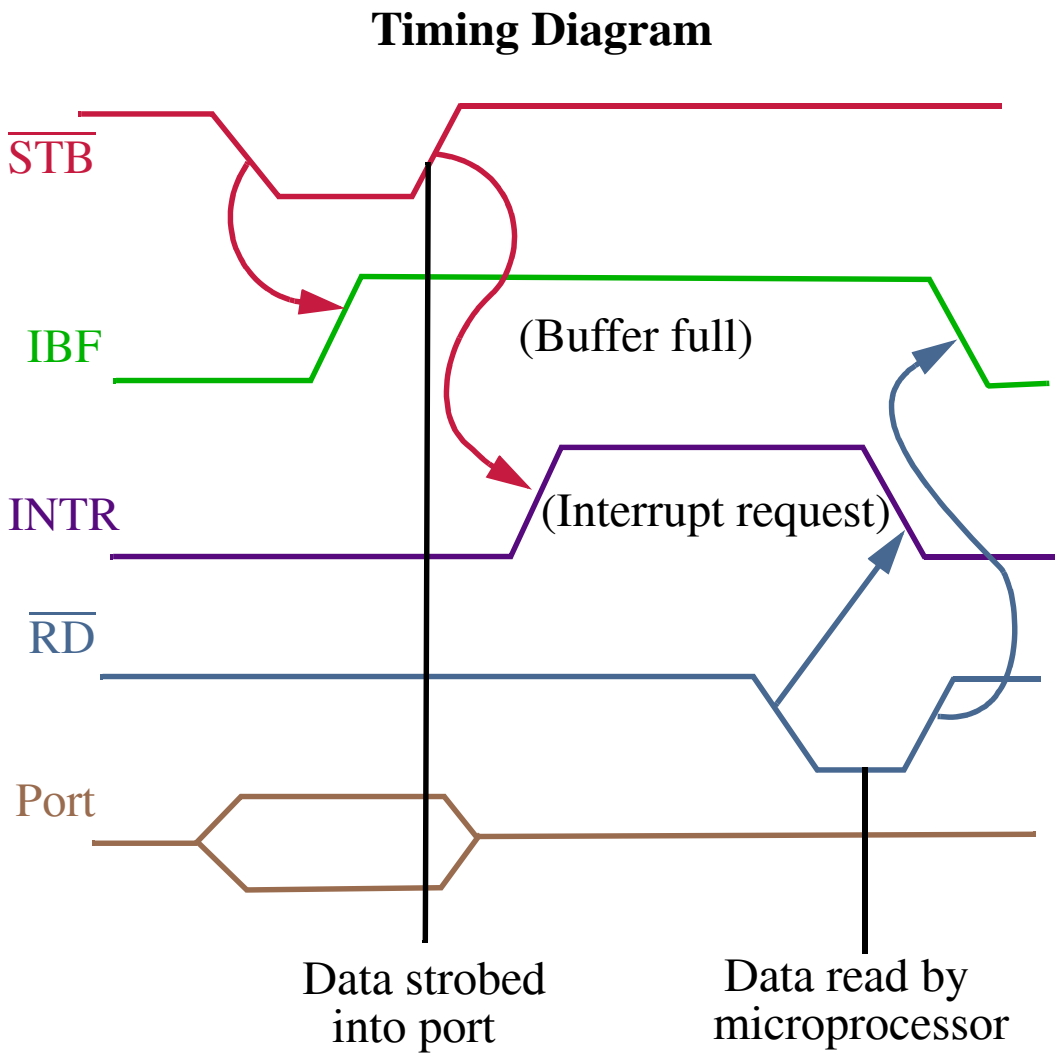
Port C used for control or handshaking signals (cannot be used for data).

Signal definitions for Mode 1 Strobed Input

$\overline{\text{STB}}$	The **strobe** input loads data into the port latch on a 0-to-1 transition
IFB	**Input buffer full** is an output indicating that the input latch contain information
INTR	**Interrupt request** is an output that requests an interrupt
INTE	The **interrupt enable signal** is neither an input nor an output; it is an internal bit programmed via the PC4(port A) or PC2(port B) bits.
PC7,PC6	The port C pins 7 and 6 are general-purpose I/O pins that are available for any purpose.

82C55: Mode 1 Strobed Input





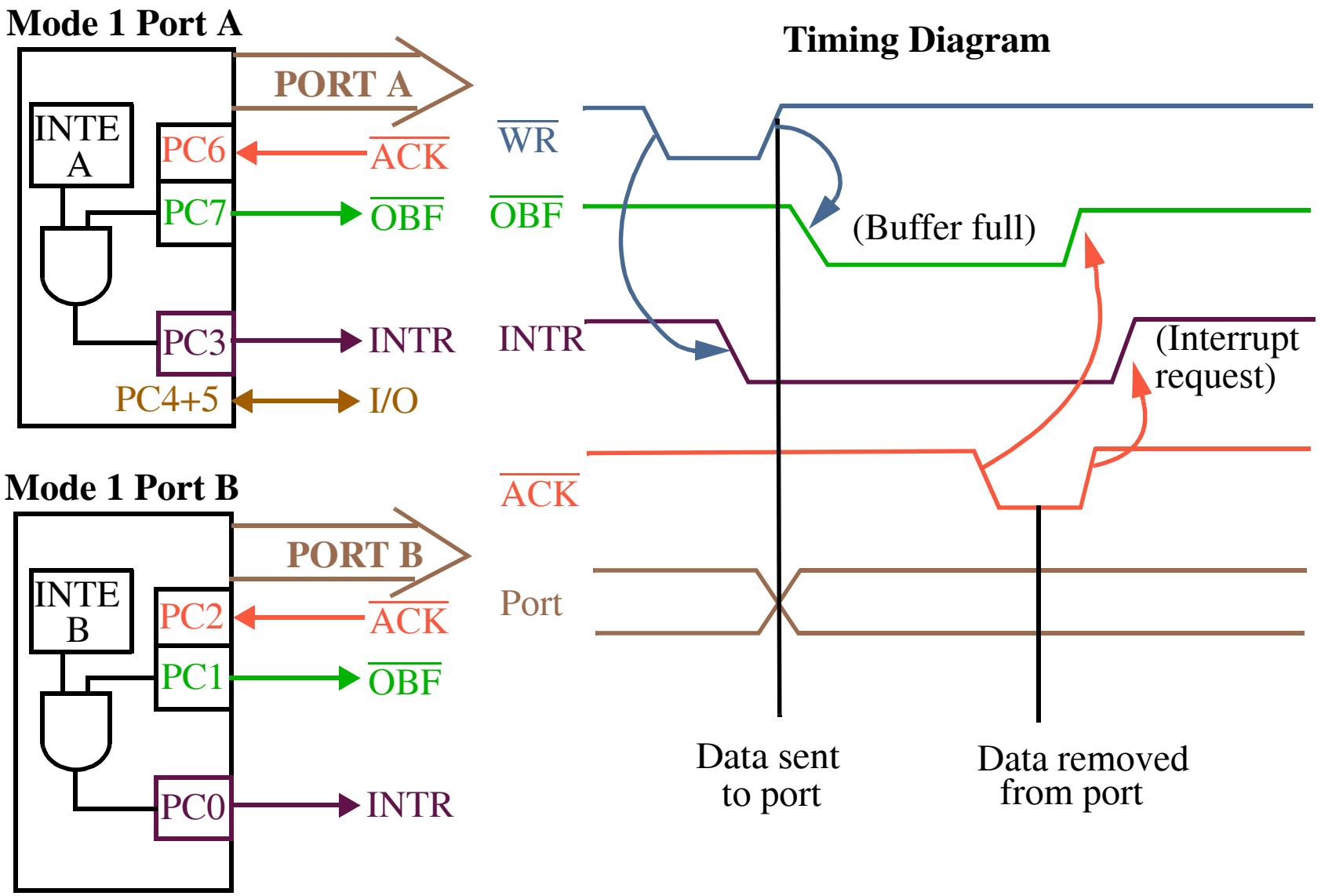
82C55: Mode 1 Strobed Output

Similar to Mode 0 output operation, except that handshaking signals are provided using port C.

Signal Definitions for Mode 1 Strobed Output

$\overline{\text{OBF}}$	**Output buffer full** is an output that goes low when data is latched in either port A or port B. Goes low on $\overline{\text{ACK}}$.
$\overline{\text{ACK}}$	The **acknowledge** signal causes the $\overline{\text{OBF}}$ pin to return to 0. This is a response from an external device.
INTR	**Interrupt request** is an output that requests an interrupt
INTE	The **interrupt enable signal** is neither an input nor an output; it is an internal bit programmed via the PC6(port A) or PC2(port B) bits.
PC5,PC4	The port C pins 5 and 4 are general-purpose I/O pins that are available for any purpose.

82C55: Mode 1 Strobed Output

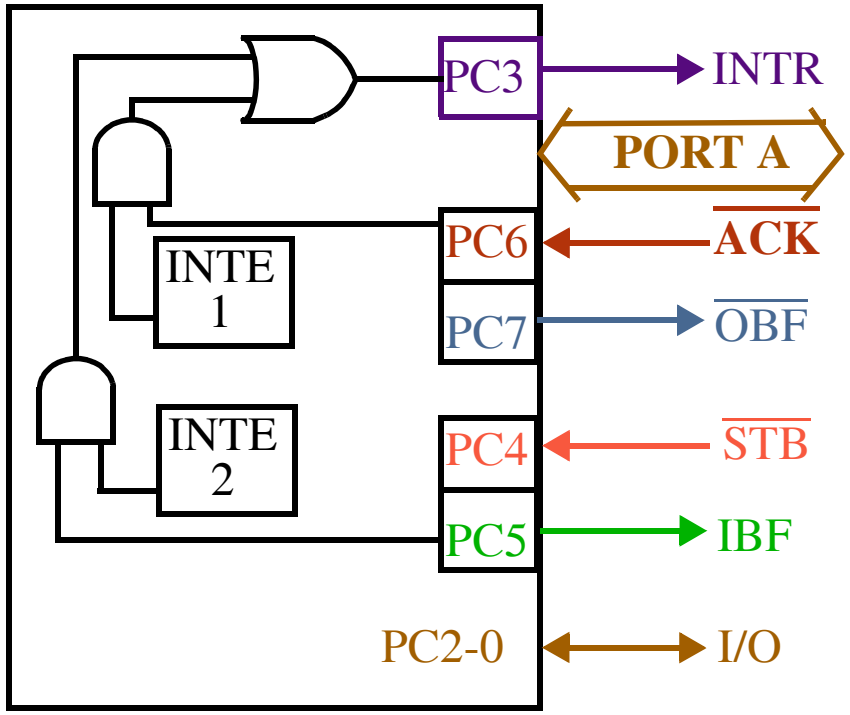


82C55: Mode 2 Bi-directional Operation

Only allowed with port A. Bi-directional bused data used for interfacing two computers, GPIB interface etc.

INTR	**Interrupt request** is an output that requests an interrupt
$\overline{\text{OBF}}$	**Output buffer full** is an output indicating that the output buffer contains data for the bi-directional bus
$\overline{\text{ACK}}$	**Acknowledge** is an input that enables tri-state buffers which are otherwise in their high-impedance state
$\overline{\text{STB}}$	The strobe input loads data into the port A latch
IFB	**Input buffer full** is an output indicating that the input latch contains information for the external bi-directional bus
INTE	**Interrupt enable** are internal bits that enable the INTR pin. Bit PC6(INTE1) and PC4(INTE2)
PC2,PC1 and PC0	Theses port C pins are general-purpose I/O pins that are available for any purpose.

82C55: Mode 2 Bi-directional Operation



Timing diagram is a combination of the Mode 1 Strobed Input and Mode 1 Strobed Output Timing diagrams.