CMPE 310 Hardware Project Spring 2008
8086 Board Design Project

Assigned: Friday, Apr. 4
Due: Friday, Apr. 25

Project Description:

Design a 8086 microprocessor board using Orcad Capture and Layout. Draw the schematic using Capture, export the necessary files for Layout and design the board using Layout. You will be required to submit the schematic and the board layouts. Your report should include the block diagram of the whole system, describe the necessary decoding details, describe the chips used in the project and their programming details (give example code fragments to setup various chips along with their port addresses) and describe the pin-outs of all headers used to connect other devices/boards to your microprocessor board. A portion of your grade will depend on the write-up. Your write-up should be a technical document, that can be used by others to use your board. Think of the write-up as the only documentation customers of your product (microprocessor board) are going to get. They should be able to understand your design and should be able to do either of the following:

• Design a similar board using information in your document, or
• Use your microprocessor board for designing a system. They should be able to understand the interface, the specifications and the programming aspects of your board to do this.

Assume that they have access to the data sheets, so don't just blindly reproduce information from the data sheets. You can point the user to the relevant data sheet for more information that is not directly related to your board, e.g. all possible programming modes of the 8279, 8255 etc. Your write-up should have a section for each of the major design blocks. Examples would be a section for the 8255, one for 8279, one for 8259, a section for the 8086 and it's associated bus logic, one for the decoding section and so on. Remember this is not a two page lab write-up, your report should have a cover page with the names of the team members and a table to contents. Include the full schematic at the end of the report as a section, reference the schematic as required in your write-up and include the Bill of Materials report from the schematic tool. Include the layout, one figure per board layer, the drill layer and the silkscreen. The silkscreen should be intuitive so as to make the soldering of components easy and important information should be visible to the user once the parts have been soldered onto the board.

You will work on this project as teams, so appoint a point of contact per team to communicate project updates or problems to me or the TA. Nobody is a team leader and you are all welcome to ask questions regarding any specific problems you might encounter. You should cooperate

with each other and meet the deadlines you have set for various design components. Divide the work equally among the team members, include a page in your report explaining the break-up of work between various team members. All of you should participate in the write-up process. You have to write the sections pertaining to the design blocks that you are assigned. Decide a common writeup format before hand so that integration of various subsections does not require major formatting edits.

Project Details:

Your design should include the following:

• 8086 in minimum mode and it's associated bus buffering/demultiplexing logic. NMI should be connected to a push-button switch with appropriate timing logic. The data bus, address bus and all control signals should be connected to headers after buffering and demultiplexing for external access to design expansion boards.

• 256KB of CMOS flash composed of 128K x 8 28F010 CMOS Flash Memory, decoded into two banks, highest address FFFFFH.

• 128KB of SRAM composed of 32K x 8 CY7C199 Static SRAM, decoded into two banks, lowest address 00000H.

• 8284A Clock Generator along with crystal and reset subcircuits

• 3 8255 chips, decoded at the following addresses (all in hex), all port connections should be pulled to headers for external access.

PPI 1: Port addresses 000F (control register), 000D, 000B, 0009

PPI 2: Port addresses 000E (control register), 000C, 000A, 0008

PPI 3: Port addresses 0007 (control register), 0005, 0003, 0001

• 1 8259 decoded at FFF6 (command) and FFF4 (data). IR0 connected to a push button switch with necessary circuits, IR1 connected to 8254 counter 2 output, IR2 connected to the 8279 IRQ output and IR3 connected to the 16550 INTR output. All other IR lines connected to headers for external access.

• 1 8254 decoded at FFDE (command), FFDC, FFDA, FFD8, with all counter 1 and counter 3 pins connected to headers. Counter 2 output connected to IR1 of the 8259, gate and clock connected to header.

• 1 8254 decoded at FFEE (command), FFEC, FFEA, FFE8, with all counter 1, 2 and counter 3 pins connected to headers.

• 1 8279 decoded at 00F2 (command) and 00F0 (data) which will be operated in the decoded mode. Connect 16 push button switches connected as four rows and four columns. Also

connect two switches to the control and shift inputs. In your layout arrange these 18 keys as well as reset, switch connected to the IR0 input on the 8259 and NMI keys to form a 5x5 keyboard matrix layout (four keys unused). CLK input to the 8279 should be the PCLK signal from the 8284A.

• 1 16550 UART decoded in the high bank at odd port address from 00EF to 00E1. The clock input to the UART should be PCLK from the 8284A and the INTR output should be connected to IR3 of the 8279. Make the connections for serial port using a MAX 235 line driver/receiver and a DSUB-9 connector. Enable all receiver inputs on the MAX 235.

• 1 20 character x 4 line LCD display with no back-light and an integrated LCD controller decoded at addresses 00D6, 00D4, 00D2 and 00D0.

• 2 common-anode 7-seg LEDs with a decimal point segment connected to 74374 latches decoded at 00CE and 00CF, 8 LEDs connected to a 74374 latch decoded at 00CC.

• 8 DIP switches connected to a 74244 decoded at 00CA.

• A power terminal block to provide power to the board. A 100uF decoupling capacitor should be connected next to the power terminal block. Place a 0.1uF decoupling capacitor next to each of the major chips in your project.

• Other misc. components that are required for the above circuits e.g. resistor packs, caps, etc. You can use discrete gate ICs, 3-to-8 decoder, 2-to-4 decoder or 16L8 (preferable) for decoding various addresses. Include the 16L8 programs if you decided to use them for decoding. Consider using the least number of chips required to perform IO and memory decoding.

Submission:

Detailed instructions on what and how to submit will be provided during the discussion sessions. The tools required for the project will be demonstrated in the discussion sessions over the next two weeks. Datasheets for the parts used in the project are posted on the class webpage for your reference.

Breakup of points:

Design Schematic and Board Layout: 70%
Documentation: 30%

Project Updates:

Any updates to the description will be minor and will be discussed in class and posted along with this document.