## Simulation with Cadence Analog Design Environment

Analog Design Environment (ADE) is integrated on Cadence Custom IC Design software. You can simulate your design (schematic, extracted layout etc.) using the ADE.

This tutorial explains necessary steps required in preparing your design and using ADE to simulate the circuit. The tutorial assumes that you have the inverter cell with schematic and symbol views created as described in "Virtuoso Schematic Composer Tutorial" (available on class website).

### **Simulation Cell View Preparation**

The first step is to prepare the simulation schematic view. In this tutorial, we will simulate the inverter using pulse voltage source connected at its input. First, create new schematic view, go to **File** -> **New** -> **Cell View**, we will call this cell **inv\_sim** as shown in Figure 1.

	New File	×
File		
Library	cmpe315	
Cell	inv_sim	
View	schematic	
Туре	schematic 🔽	
Application		_
Open with	Schematics L	
Always use th	is application for this type of file	
Library path file		
u/users/r/a/r	ahman2/home/cadence_ic6/cds	s.lib
	OK Cancel	Help

Figure 1: New simulation cell view

Next, we need to place the symbol of inverter on the schematic. Create new instance of the inverter by select "**inv**" from "**cmpe315**" library from the component browser as shown in Figure 2. At the Add Instance dialog, make sure you have **symbol** selected as shown in Figure 3, if not you can manually type in or click Browse.

Create instances of vdd, gnd, vdc and vpulse, create new OUTPUT pin (with "output" direction) and then make appropriate connections as shown in Figure 4. You can find vdc and vpulse from Voltage\_Sources -> vdc, Voltage\_Sources -> vpulse in NCSU\_Analog\_Parts library.

Add Instance >				
Library	cmpe315	Browse		
Cell	inv		1	
View	symbol			
Names				
🗹 Add Wir	e Stubs at: O all ter	minals  e registered terminals only		
Array	R	ows 1 Columns 1		
	🔔 Rotate	🚺 Sideways 🚭 Upside Down		
		Hide Cancel Defaults He	lp)	

Figure 2: Select inv (inverter) cell from Component Browser

	Add Instance	×
Library	cmpe315 Browse	
Cell	inv	
View	symbol	
Names		
🗹 Add Wir	e Stubs at: all terminals  registered terminals only	
Array	Rows 1 Columns 1	
	🖹 Rotate 🛛 🕼 Sideways 🛛 🚭 Upside Down	
	Hide Cancel Defaults He	elp )

Figure 3: Select symbol view of inv cell



Figure 4: Schematic of inv\_sim

#### CMPE 315/CMPE640 UMBC

### Simulation with Analog Design Environment Tutorial

Now, we need to change the properties of vdc and vpulse. To change the property, click on the component and go to **Edit -> Properties -> Objects**. For vdc, set DC voltage to 5V as shown in Figure 5. For vpulse, set Voltage1 to 0V, Voltage2 to 5V, Delay time to 1ns, rise and fall times to 500ps, pulse width to 5ns and period to 10.1ns as shown in Figure 6.

	Edit Object Properties ×					
Apply To Show	Apply To Only current I instance I Show System I user I CDF					
В	rowse	Reset Insta	nce Labels Di	isplay		
Property	/		Value		Display	
Library Na	ame 🚺	NCSU_Analog_	Parts		off	
Cell Name	• •	/dc			off 🔽	
View N arr	ne s	symbol			off 🔽	
Instance N	Name 🚺	/1			off 🔽	
		Add	Delete	Modify	)	
User Pro	operty	Master Val	ue	Local Value	Display	
lvsignore	e [1	TRUE			off 🔽	
CDF Para	ameter		Value		Display	
AC magnitude					off 🔽	
AC phase					off	
DC voltage		5 V			off 🔽	

Figure 5: Property of vdc used for the simulation

AC magnitude		off 🔽
AC phase		off
Voltage 1	0 V	off 🔽
Voltage 2	5 V	off 🔽
Delay time	1n s	off 🔽
Rise time	500p s	off 🔽
Fall time	500p s	off 🔽
Pulse width	5n s	off 🔽
Period	10.1n s	off 🔽
DC voltage		off 🔽

Figure 6: Property of vpulse used for the simulation

## **Hierarchy Editor**

Hierarchy Editor lets you change views of the cell for simulation. For example, if you have made the schematic and layout for the inverter, you can create only one simulation view and then switch between schematic or extracted layout in the simulation using Hierarchy Editor. You can also mix multiple view types of cells in simulation using Hierarchy Editor (This mean you can simulate schematic of adder connects to layout of multiplier and/or vhdl of control logic).

To create new Hierarchy Editor view, highlight inv\_sim cell in Library Manager, go to **File -> New -> Cell View** and select type as config as shown in Figure 7.

	New File	×
File		
Library	cmpe315	
Cell	inv_sim	
View	config	
Туре	config	J
Application		_
Open with	Hierarchy Editor	
Always use th	is application for this type of file	
Library path file		
u/users/r/a/r	ahman2/home/cadence_ic6/cds	.lib
	OK Cancel	lelp )

Figure 7: New Hierarchy Editor view

The New Configuration dialog will show up, click **view** and select schematic of inv\_sim as the top cell as shown in Figure 8. Then click **Use Template**, another dialog will appear as shown in Figure 9, select **spectre** template and click OK. At View List, add "**extracted structural schematic**" separated by spaces exactly as shown in Figure 10. Click OK to close New Configuration dialog.

Now you will see Hierarchy Editor dialog as shown in Figure 11. From here, you can specify view you want to use in the simulation. For us, we will use schematic view of inverter in the simulation, so type in **schematic** in **View to Use** column of **inv** cell as shown in the figure. Click  $\blacksquare$  icon to save the configuration and then close the Hierarchy Editor.

	New Configuration	;
Top Cell		
Library	cmpa315	1
Collo		
Cell:		H
View:	schematic	
Global Bin	dings	
Library Lis	t:	)
View List:		
Stop List:		
Constraint	List:	)
Descriptio		
1		
	OK Cancel Use Template Help	

Figure 8: New Configuration

	Use Template	×
Template		
Name:	spe ctre	
From File:	stalls/IC617/share/cdssetup/hierEditor/templates/spectre	1].
	OK Cancel Apply Help	

Figure 9: Use Template

	New Configuration	×
Top Cell		
Library: c	mpe315	
Cell: ir	nv_sim	
View:	nyView	
Global Bindi	ings Add Here	
Library List:	myLib	
View List:	chematic veriloga ahdl pspice extracted structural schematic	
Stop List:	spectre	

Figure 10: Add "extracted structural schematic" to View List

Vi	rtuoso® Hierarchy	Editor: New Config	juration (Save l	Needed)	×
Launch <u>File E</u> dit <u>V</u> iew	<u>H</u> elp			cād	епсе
<u>                                     </u>	) 🥱 🥐 🕕 🖬	🤞 🗋 🖻 🔍	earch 🔽	✓ Ø Update Nee ded	
Top Cell		? <b>-</b> ×	Global Bindings	i	? 🗗 🗙
Library: cmpe315			Library List:	myLib	
Cell: inv_sim			View List:	ematic veriloga ahdl pspice	
View: schematic			Stop List:	spectre	
Open Edit	ADE L	ADE Explorer	Constraint List:		
Table View Tree View					
Cell Bindings					
Library	Cell	View Found	View To Us	e Inherited View Li	st
NCSU_Analog_Parts	nmos4	spe ctre		spectre cmos_sch c	m
NCSU_Analog_Parts	pmos4	spe ctre		spectre cmos_sch c	m
analogLib	vdc	spectre		spectre cmos_sch c	m
analogLib	vpulse	spectre		spectre cmos_sch c	m
cmpe315	inv	schematic	schematic	spectre cmos_sch c	m
cmpe315	inv_sim	schematic		spectre cmos_sch c	m

Figure 11: Hierarchy Editor

## **Open Analog Design Environment (ADE)**

Open the config view of inv\_sim cell (by double clicking) from Library manager, the dialog as shown in Figure 12 will show up, click OK. The schematic of inv\_sim should be opened, go to **Launch -> ADE L** from the Hierarchy editor window. The ADE window should appear as shown in Figure 13.



Figure 12: Open config view

ADE L	(2) - cmpe315 inv_sim sch	hematic	×
Launch Session Setup Analyses Variables	<u>O</u> utputs <u>S</u> imulation <u>R</u> esults	<u>T</u> ools <u>H</u> elp	cādence
[ 🚰 🔊 🍞 25.0 🛛 🔊 🎾 🏠	🗹 🗁		
Design Variables	Analyses		? 🗗 🗙 🔐
Name Value	Type Enable	Arguments	Trans
			18
			×
	Outputs		? 8 × 💛
	Name/Signal/Expr	Value Plot Save Save Op	otions 🔤 🎶
	ļ		
>	Plot after simulation: Auto	Plotting mode: Replace	
7(14) Stimuli		Status: Ready   T=25.0 C   Simul	ator: hspiceD 📗

Figure13: Analog Design Environment

### **Simulation Setup**

Go to **Simulator -> Directory -> Host**. Then select **Spectre** as a simulator as shown as Figure 14 (c).

Then, we have to set up the model libraries of the NMOS and PMOS. Go to **Setup -> Model library** then browse to these model files as shown in Figure 14 (b)

#### <u>/afs/umbc.edu/software/cadence/design\_kits/ncsu-cdk-1.6.0.beta/models/spectre/</u> /standalone/ami06N.m

#### <u>/afs/umbc.edu/software/cadence/design\_kits/ncsu-cdk-1.6.0.beta/models/spectre/</u> standalone/ami06P.m

Next, we need to set the type of analysis, stop time and accuracy level for the simulation. Go to **Analyses -> Choose**, the Choosing Analyses dialog will appear. Select **tran** for analysis type, enter **25n** (run simulation for 25ns) for stop time, click on **conservative** for accuracy mode and **Enabled** to enable this simulation setup as shown in Figure 14 (a).

Choosing Analyses ADE L (4)					×	
Analysis	<ul> <li>tran</li> <li>xf</li> <li>stb</li> <li>pss</li> <li>pxf</li> <li>qpnoise</li> <li>hbac</li> </ul>	<ul> <li>dc</li> <li>sens</li> <li>pz</li> <li>pac</li> <li>psp</li> <li>qpxf</li> <li>hbstb</li> </ul>	<ul> <li>ac</li> <li>dcmatch</li> <li>sp</li> <li>pstb</li> <li>qpss</li> <li>qpsp</li> <li>hbnoise</li> </ul>	<ul> <li>noise</li> <li>acmatch</li> <li>envlp</li> <li>pnoise</li> <li>qpac</li> <li>hb</li> <li>hbsp</li> </ul>		
	⊖ hbxf	Fransient A	nalysis			
Stop Time Accuracy D Conse	Stop Time 25n Accuracy Defaults (errpreset)					
Dynamic Parameter						
Chabled Options						

*(a)* 

#### Figure 14 : Choosing Analyses

hspiceD2: Model Library Setup					
Model File       Section         □       Global Model Files         □       ✓e/cadence/de sign_kits/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06N.m         ✓ dence/design_kits/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06P.m         ✓ dence/design_kits/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06P.m         ✓ dence/design_kits/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06P.m         ✓ dence/design_kits/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06P.m					
OK Cancel Apply	<u>H</u> elp				

*(b)* 

Figure 14 : Setting up the Model library.

Choosing Simulator/Directory/Host ADE L (4) ×				
Simulator	spectre			
Project Directory	/afs/umbc.edu/users/r/a/rahman2/home/cadence/simula1			
Host Mode	🧕 local 🔾 remote 🔾 distributed			
Host				
Remote Directory				
	OK Cancel Defaults Apply He	elp )		

*(c)* 

Figure 14 : Selecting Spectre as the simulator.

Next, we will select signals we want to observe after run simulation. Go to **Outputs** -> **To Be Plotted** -> **Select On Design**. Click on wires/nets on schematic that you want to observe. In our case, click wire connected to INPUT and OUTPUT of the inverter. The ADE window after having analyses and outputs setup is shown in Figure 15.

	ADE L (4) - cmpe315 inv_sim schematic							×				
Laund	n S <u>e</u> ssion	Setup	<u>A</u> nalyses	<u>V</u> aria bles	<u>O</u> utputs	<u>S</u> imulation	n <u>R</u> esults	<u>T</u> ools	<u>H</u> elp		cād	ence
11 📇 1	•٦   😪	27	] 🔊 ⊁	• 🖄 (	🛃 🗁						_	
Design	Variables				Analys	es		_		_	? 8	× AC
	Name		Value		Туре	Enable	0.255 cons	an esti es	Argun	nents		Trans
					1 tran	⊻	0 ZSH COHS	ervauve				10
												×
												0
					Outout	te			_		7 8	x 🖸
					o utpu	vame/Signal	/Expr	Value	Plot	Save	Save Options	W
					1 OUTPU	л			<b>_</b>		allv	
					2 net3				<b>V</b>		allv	
					1							
					Plot after	simulation:	Auto		Plotting	mode:	Replace	ī I
> Sele	ct on Schem	atic Out	puts to Be F	Plotted	riocartei	sinaation.		_	roung	, mode.		
9(16)	Model Libra	aries			9	Status: Selec	ting outputs	to be pl	otted	T=27	C Simulator: sp	ectre 📗

Figure 15: ADE after analyses and outputs setup

Go to **Simulation -> Netlist -> Create**, the final netlist will appear as shown in Figure 16. If the netlist does not show up, see if there are any errors on CIW window or go to **Simulation -> Output Log**. (Note that this step may be skipped but we recommend you to run if you are setting the new simulation for the new cell.)

/afs/umbc.edu/users/r/a/rahman2/home/cadence/simulation/inv\_sim... × File Edit View Help cādence // Generated for: spectre // Generated on: Aug 23 16:46:36 2017 // Design library name: cmpe315 // Design cell name: inv\_sim // Design view name: schematic simulator lang=spectre global 0 vdd! include "/afs/umbc.edu/software/cadence/design\_kits/ncsu-cdk-1.6.0.beta/mod include "/afs/umbc.edu/software/cadence/design\_kits/ncsu-cdk-1.6.0.beta/mod // Library name: cmpe315 // Cell name: inv // View name: schematic subckt inv INPUT OUTPUT N0 (OUTPUT INPUT 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 \ ps=6u pd=6u m=1 region=sat P0 (OUTPUT INPUT vdd! vdd!) ami06P w=1.5u 1=600n as=2.25e-12 \ ad=2.25e-12 ps=6u pd=6u m=1 region=sat ends inv // End of subcircuit definition. // Library name: cmpe315 // Cell name: inv\_sim // View name: schematic I1 (net3 OUTPUT) inv V0 (net3 0) vsource type=pulse val0=0 val1=5 period=10.1n delay=1n \ rise=500p fall=500p width=5n V1 (vdd! 0) vsource type=dc dc=5 simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \ tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \ checklimitdest=psf tran tran stop=25n errpreset=conservative write="spectre.ic" \ writefinal="spectre.fc" annotate=status maxiters=5 finalTimeOP info what=oppoint where=rawfile modelParameter info what=models where=rawfile element info what=inst where=rawfile outputParameter info what=output where=rawfile designParamVals info what=parameters where=rawfile primitives info what=primitives where=rawfile subckts info what=subckts where=rawfile sa<u>veOptions options save=allpub</u> HelpAction 22 L1 C1

Figure 16: Created Final Netlist

#### **Run Simulation**

Now run the simulation, go to **Simulation** -> **Run**. If the circuit is large, it might take times for the simulation to finish (depends on the size of the circuit, might take from few minutes to many hours). The information on running simulation is displayed on CIW window.

#### **Simulation Results on Waveform Window**

After the simulation is finished, the waveform window will show up as shown in Figure 17. All signals selected will plotted on the same axes and difficult to look at some time. Go to **Graph -> Split current Strip** to have waveforms plotted on separate axes as shown in Figure 18.

#### CMPE 315/CMPE640 UMBC

#### Simulation with Analog Design Environment Tutorial









Figure 18: Waveform Window after Strip

## **Save State**

You can save simulation setting so that next time you open ADE you do not need to setup Analyses and Output to be plotted (and any other settings) again. Go to **Session** -> Save State, enter state name as shown in Figure 19 and then click OK.

-	×		
Save State Option	ا پ	Directory 🔾 Cellview	<u>^</u>
Directory Options			
State Save Directory	~/.artist_	states	Browse
Save As	state1		=
Existing States			

#### Figure 19: Save State

# Load State

To load saved state, go to **Session -> Load State**, select the state you want to load from the list as shown in Figure 20.

	Loading State ADE L (4)		×
Load State Option	Oirectory Cellview		Â
Directory Options			-
State Load Directory	~/.artist_states	Browse	
Library	cmpe315 🔽		=
Cell	inv_sim 🔽		
Simulator	spe ctre 🔽		
State Name	state1	T	

Figure 20: Load State

### Save image from Waveform Window

You can save image of the waveform window by going to **File** -> **Save image**, the Save Image dialog as shown in Figure 21 will appear.Click on the **Directory bar** and set a directory to save the image file (You can set your save directory as per your liking.) Then put your desried directory in the Address bar, Type **plot** (You can give your desired name for the image file) in **File name**, select type as **PNG**. Finally click on **Save** in the window to save the image in your desired directory.



Figure 21: Save Image