S6A0069

40 SEG / 16 COM DRIVER & CONTROLLER FOR DOT MATRIX LCD

Ver. 0.0

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INTRODUCTION

S6A0069 is a dot matrix LCD driver & controller LSI which is fabricated by low power CMOS technology. It can display 1, 2-line with 5 x 8 or 5 x 11 dots format.

FUNCTIONS

- Character type dot matrix LCD driver & controller.
- Internal driver: 16 common and 40 segment signal output.
- Easy interface with 4-bit or 8-bit MPU
- Display character pattern: 5 x 8 dots format (204 kinds), 5 x 11 dots format (32 kinds)
- The special character pattern can be programmable by Character Generator RAM directly.
- A customer character pattern can be programmable by mask option.
- It can drive a maximum 80 characters by using the S6A0065 or S6A2067 externally.
- Various instruction functions
- Automatic power on reset

FEATURES

- Internal Memory
  - Character Generator ROM (CGROM): 10,080 bits (204 characters x 5 x 8 dot) & (32 characters x 5 x 11 dot)
  - Character Generator RAM (CGRAM): 64 x 8 bits (8 characters x 5 x 8 dot)
  - Display Data RAM (DDRAM): 80 x 8 bits (80 characters max.)
- Low Power Operation
  - Power supply voltage range: 2.7 to 5.5V ($V_{DD}$)
  - LCD drive voltage range: 3.0 to 13.0V ($V_{DD}$ - $V_5$)
- CMOS process
- Programmable duty cycle: 1/8, 1/11, 1/16
- Internal oscillator with an external resistor
- Low power consumption
- Bare chip available
PAD CONFIGURATION

Chip size: 4060 × 3840
Pad size: 100 × 100
Unit: μm
# PAD CENTER COORDINATES

Unit: um

<table>
<thead>
<tr>
<th>PAD NUM.</th>
<th>PAD NAME</th>
<th>COORDINATE</th>
<th>PAD NUM.</th>
<th>PAD NAME</th>
<th>COORDINATE</th>
<th>PAD NUM.</th>
<th>PAD NAME</th>
<th>COORDINATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>S22</td>
<td>-1864 1465</td>
<td>28</td>
<td>V3</td>
<td>-670 -1754</td>
<td>55</td>
<td>C9</td>
<td>1864 335</td>
</tr>
<tr>
<td>2</td>
<td>S21</td>
<td>-1864 1340</td>
<td>29</td>
<td>V4</td>
<td>-520 -1754</td>
<td>56</td>
<td>C10</td>
<td>1864 460</td>
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<td>3</td>
<td>S20</td>
<td>-1864 1215</td>
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<td>C11</td>
<td>1864 585</td>
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<td>4</td>
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<td>-1864 1090</td>
<td>31</td>
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<td>58</td>
<td>C12</td>
<td>1864 710</td>
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<td>5</td>
<td>S18</td>
<td>-1864 965</td>
<td>32</td>
<td>CLK2</td>
<td>-70 -1754</td>
<td>59</td>
<td>C13</td>
<td>1864 835</td>
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<td>6</td>
<td>S17</td>
<td>-1864 840</td>
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<td>VDD</td>
<td>80 -1754</td>
<td>60</td>
<td>C14</td>
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<td>7</td>
<td>S16</td>
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<td>M</td>
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<td>61</td>
<td>C15</td>
<td>1864 1085</td>
</tr>
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<td>8</td>
<td>S15</td>
<td>-1864 590</td>
<td>35</td>
<td>D</td>
<td>380 -1754</td>
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<td>C16</td>
<td>1864 1210</td>
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<tr>
<td>9</td>
<td>S14</td>
<td>-1864 465</td>
<td>36</td>
<td>RS</td>
<td>518 -1754</td>
<td>63</td>
<td>S40</td>
<td>1864 1341</td>
</tr>
<tr>
<td>10</td>
<td>S13</td>
<td>-1864 340</td>
<td>37</td>
<td>R/W</td>
<td>642 -1754</td>
<td>64</td>
<td>S39</td>
<td>1864 1466</td>
</tr>
<tr>
<td>11</td>
<td>S12</td>
<td>-1864 215</td>
<td>38</td>
<td>E</td>
<td>768 -1754</td>
<td>65</td>
<td>S38</td>
<td>1864 1574</td>
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<tr>
<td>12</td>
<td>S11</td>
<td>-1864 90</td>
<td>39</td>
<td>DB0</td>
<td>894 -1754</td>
<td>66</td>
<td>S37</td>
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<tr>
<td>13</td>
<td>S10</td>
<td>-1864 -35</td>
<td>40</td>
<td>DB1</td>
<td>1018 -1754</td>
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<td>14</td>
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<td>DB2</td>
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<td>1864 1754</td>
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<td>15</td>
<td>S8</td>
<td>-1864 -285</td>
<td>42</td>
<td>DB3</td>
<td>1864 -1362</td>
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<td>S34</td>
<td>1864 1754</td>
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<tr>
<td>16</td>
<td>S7</td>
<td>-1864 -410</td>
<td>43</td>
<td>DB4</td>
<td>1864 -1238</td>
<td>70</td>
<td>S33</td>
<td>1864 1754</td>
</tr>
<tr>
<td>17</td>
<td>S6</td>
<td>-1864 -535</td>
<td>44</td>
<td>DB5</td>
<td>1864 -1112</td>
<td>71</td>
<td>S32</td>
<td>1864 1754</td>
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<tr>
<td>18</td>
<td>S5</td>
<td>-1864 -660</td>
<td>45</td>
<td>DB6</td>
<td>1864 -988</td>
<td>72</td>
<td>S31</td>
<td>1864 1754</td>
</tr>
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<td>19</td>
<td>S4</td>
<td>-1864 -785</td>
<td>46</td>
<td>DB7</td>
<td>1864 -862</td>
<td>73</td>
<td>S30</td>
<td>1864 1754</td>
</tr>
<tr>
<td>20</td>
<td>S3</td>
<td>-1864 -910</td>
<td>47</td>
<td>C1</td>
<td>1864 -665</td>
<td>74</td>
<td>S29</td>
<td>1864 1754</td>
</tr>
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<td>21</td>
<td>S2</td>
<td>-1864 -1034</td>
<td>48</td>
<td>C2</td>
<td>1864 -540</td>
<td>75</td>
<td>S28</td>
<td>1864 1754</td>
</tr>
<tr>
<td>22</td>
<td>S1</td>
<td>-1864 -1159</td>
<td>49</td>
<td>C3</td>
<td>1864 -415</td>
<td>76</td>
<td>S27</td>
<td>1864 1754</td>
</tr>
<tr>
<td>23</td>
<td>GND</td>
<td>-1864 -1285</td>
<td>50</td>
<td>C4</td>
<td>1864 -290</td>
<td>77</td>
<td>S26</td>
<td>1864 1754</td>
</tr>
<tr>
<td>24</td>
<td>OSC1</td>
<td>-1864 -1414</td>
<td>51</td>
<td>C5</td>
<td>1864 -165</td>
<td>78</td>
<td>S25</td>
<td>1864 1754</td>
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<tr>
<td>25</td>
<td>OSC2</td>
<td>-1120 -1754</td>
<td>52</td>
<td>C6</td>
<td>1864 -40</td>
<td>79</td>
<td>S24</td>
<td>1864 1754</td>
</tr>
<tr>
<td>26</td>
<td>V1</td>
<td>-970 -1754</td>
<td>53</td>
<td>C7</td>
<td>1864 85</td>
<td>80</td>
<td>S23</td>
<td>1864 989</td>
</tr>
<tr>
<td>27</td>
<td>V2</td>
<td>-820 -1754</td>
<td>54</td>
<td>C8</td>
<td>1864 210</td>
<td></td>
<td></td>
<td></td>
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</table>
## PIN DESCRIPTION

<table>
<thead>
<tr>
<th>PIN</th>
<th>No</th>
<th>I/O</th>
<th>NAME</th>
<th>DESCRIPTION</th>
<th>INTERFACE</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>33</td>
<td></td>
<td>Supply Voltage</td>
<td>Supply Voltage for logical circuit (+3V ± 10%, +5V ± 10%)</td>
<td>Power Supply</td>
</tr>
<tr>
<td></td>
<td>23</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>26-30</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td></td>
<td></td>
<td>0V (GND)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V1 - V5</td>
<td>26-30</td>
<td></td>
<td>Bias voltage level for LCD driving.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S1 - S40</td>
<td>1-22, 63-80</td>
<td>O</td>
<td>Segment output</td>
<td>Segment signal output for LCD drive.</td>
<td>LCD</td>
</tr>
<tr>
<td>C1 - C16</td>
<td>47-62</td>
<td>O</td>
<td>Common output</td>
<td>Common signal output for LCD drive.</td>
<td>LCD</td>
</tr>
<tr>
<td>OSC1</td>
<td>24</td>
<td>I</td>
<td>Oscillator</td>
<td>When use internal oscillator, connect external Rf resistor. If external clock is used, connect it to OSC1.</td>
<td>External Resistor/Oscillator OSC1</td>
</tr>
<tr>
<td>OSC2</td>
<td>25</td>
<td>O</td>
<td>Oscillator</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLK1</td>
<td>31</td>
<td>O</td>
<td>Extension driver Latch clock</td>
<td>extension driver latch clock.</td>
<td>Extension driver</td>
</tr>
<tr>
<td>CLK2</td>
<td>32</td>
<td>O</td>
<td>Extension driver Shift clock</td>
<td>extension driver shift clock.</td>
<td>Extension driver</td>
</tr>
<tr>
<td>M</td>
<td>34</td>
<td>O</td>
<td>Alternated signal for LCD driver output</td>
<td>Outputs the alternating signal to convert LCD driver waveform to AC.</td>
<td>Extension driver</td>
</tr>
<tr>
<td>D</td>
<td>35</td>
<td>O</td>
<td>Display data interface</td>
<td>Outputs extension driver data (the 41th dot’s data)</td>
<td>Extension driver</td>
</tr>
<tr>
<td>RS</td>
<td>36</td>
<td>I</td>
<td>Register select</td>
<td>Used as register selection input. When RS = “High”, Data register is selected. When RS = “Low”, Instruction register is selected.</td>
<td>MPU</td>
</tr>
<tr>
<td>R/W</td>
<td>37</td>
<td>I</td>
<td>Read/Write</td>
<td>Used as read/write selection input. When R/W = “High”, read operation. When R/W = “Low”, write operation.</td>
<td>MPU</td>
</tr>
<tr>
<td>E</td>
<td>38</td>
<td>I</td>
<td>Read/write enable</td>
<td>Read/write enable signal.</td>
<td>MPU</td>
</tr>
<tr>
<td>DB0- DB3</td>
<td>39-42</td>
<td>I/O</td>
<td>Data bus 0-7</td>
<td>When 8-bit bus mode, used as low order bidirectional data bus. In 4-bit bus mode open these pins.</td>
<td>MPU</td>
</tr>
<tr>
<td>DB4- DB7</td>
<td>43-46</td>
<td></td>
<td></td>
<td>When 8-bit bus mode, used as high order bidirectional data bus. In case of 4-bit bus mode, used as both high and low order. DB7 is used for Busy Flag output.</td>
<td>MPU</td>
</tr>
</tbody>
</table>
FUNCTION DESCRIPTION

System Interface
This chip has all two kinds of interface type with MPU : 4-bit bus and 8-bit bus. 4-bit bus and 8-bit bus is selected by DL bit in the instruction register. During read or write operation, two 8-bit registers are used. one is data register (DR), the other is instruction register(IR). The data register(DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM. The target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. So to speak, after MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically. The instruction register (IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data. To select register, use RS input pin in 4-bit/8-bit bus mode.

<table>
<thead>
<tr>
<th>RS</th>
<th>R/W</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>Instruction Write operation (MPU writes Instruction code into IR)</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>Read Busy Flag (DB7) and address counter (DB0 - DB6)</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>Data Write operation (MPU writes data into DR)</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>Data Read operation (MPU reads data from DR)</td>
</tr>
</tbody>
</table>

Busy Flag (BF)
When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R/W = High (Read Instruction Operation), through DB7 port. Before executing the next instruction, be sure that BF is not High.

Address Counter (AC)
Address Counter(AC) stores DDRAM/CGRAM address, transferred from IR. After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1. When RS = "Low" and R/W = "High", AC can be read through DB0 - DB6 ports.
Display Data RAM (DDRAM)

DDRAM stores display data of maximum 80 x 8 bits (80 characters). DDRAM address is set in the address counter (AC) as a hexadecimal number. (refer to Figure1.)

<table>
<thead>
<tr>
<th>MSB</th>
<th>LSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC6</td>
<td>AC5</td>
</tr>
<tr>
<td>AC4</td>
<td>AC3</td>
</tr>
<tr>
<td>AC2</td>
<td>AC1</td>
</tr>
<tr>
<td>AC0</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 1. DDRAM Address**

1) 1-line Display

In case of 1 line display, the address range of DDRAM is 00H - 4FH. Extension driver will be used. Fig-2 shows the example that 40 segment extension driver is added.

**Figure 2. 1-line x 24 Character Display with 40 Segment Extension Driver**
2) 2-line Display

In case of 2 line display, the address range of DDRAM is 00H - 27H, 40H - 67H. Extension driver will be used. Figure 3 shows the example that 40 segment extension driver is added.

<table>
<thead>
<tr>
<th>DDRAM Address</th>
<th>Display position</th>
</tr>
</thead>
<tbody>
<tr>
<td>00 01 02 03 04 05 06 07</td>
<td>SEG1 S6A0069 SEG40 SEG1 Extension driver (40 SEG) SEG40</td>
</tr>
<tr>
<td>40 41 42 43 44 45 46 47</td>
<td>SEG1 Extension driver (40 SEG) SEG40</td>
</tr>
<tr>
<td>80 09 0A 0B 0C 0D 0E 0F</td>
<td>SEG1 Extension driver (40 SEG) SEG40</td>
</tr>
</tbody>
</table>

(After Shift Left)

<table>
<thead>
<tr>
<th>DDRAM Address</th>
<th>Display position</th>
</tr>
</thead>
<tbody>
<tr>
<td>01 02 03 04 05 06 07 08</td>
<td>SEG1 S6A0069 SEG40 SEG1 Extension driver (40 SEG) SEG40</td>
</tr>
<tr>
<td>41 42 43 44 45 46 47 48</td>
<td>SEG1 Extension driver (40 SEG) SEG40</td>
</tr>
<tr>
<td>89 0A 0B 0C 0D 0E 0F 10</td>
<td>SEG1 Extension driver (40 SEG) SEG40</td>
</tr>
</tbody>
</table>

(After Shift Right)

<table>
<thead>
<tr>
<th>DDRAM Address</th>
<th>Display position</th>
</tr>
</thead>
<tbody>
<tr>
<td>27 00 01 02 03 04 05 06</td>
<td>SEG1 S6A0069 SEG40 SEG1 Extension driver (40 SEG) SEG40</td>
</tr>
<tr>
<td>67 40 41 42 43 44 45 46</td>
<td>SEG1 Extension driver (40 SEG) SEG40</td>
</tr>
<tr>
<td>47 48 49 4A 4B 4C 4D 4E</td>
<td>SEG1 Extension driver (40 SEG) SEG40</td>
</tr>
</tbody>
</table>

Figure 3. 2-line x 24 Character Display with 40 Segment Extension Driver
CGROM (Character Generator ROM)
CGROM has a 5 x 8 dots 204 characters pattern and a 5 x 10 dots 32 characters pattern. CGROM has 204 character patterns of 5 x 8 dots, and 32 character patterns of 5 x 11 dots.

CGRAM (Character Generator RAM)
CGRAM has up to 5 x 8 dot, 8 characters. By writing font data to CGRAM, user defined characters can be used (refer to Table 5)

Timing Generation Circuit
Timing generation circuit generates clock signals for the internal operations.

LCD Driver Circuit
LCD Driver circuit has 16 common and 40 segment signals for LCD driving. Data from CGRAM/CGROM is transferred to 40 bit segment latch serially, and then it is stored to 40 bit shift latch. When each common is selected by 16 bit common register, segment data also output through segment driver from 40 bit segment latch. In case of 1-line display mode, COM1- COM8 have 1/8 duty or COM1 — COM11 have 1/11 duty, and in 2-line mode, COM1 - COM16 have 1/16 duty ratio.

Cursor / Blink Control Circuit
It controls cursor/blink ON / OFF at cursor position.
Table 5. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

<table>
<thead>
<tr>
<th>Character Code (DDRAM data)</th>
<th>CGRAM Address</th>
<th>CGRAM Data</th>
<th>Pattern number</th>
</tr>
</thead>
<tbody>
<tr>
<td>D7  D6 D5 D4 D3 D2 D1 D0</td>
<td>A5 A4 A3 A2 A1 A0</td>
<td>P7 P6 P5 P4 P3 P2 P1 P0</td>
<td></td>
</tr>
<tr>
<td>0  0  0  0  x  0  0  0</td>
<td>0  0  0  0  0  0  0  0</td>
<td>x  x  x  0  1  1  1  0</td>
<td>Pattern 1</td>
</tr>
<tr>
<td>.  .  .  .  .  .  .  .</td>
<td>0  0  1</td>
<td>1  0  0  0  1</td>
<td></td>
</tr>
<tr>
<td>.  .  .  .  .  .  .  .</td>
<td>0  1  0</td>
<td>1  0  0  0  1</td>
<td></td>
</tr>
<tr>
<td>.  .  .  .  .  .  .  .</td>
<td>0  1  1</td>
<td>1  1  1  1  1</td>
<td></td>
</tr>
<tr>
<td>.  .  .  .  .  .  .  .</td>
<td>1  0  0</td>
<td>1  0  0  0  1</td>
<td></td>
</tr>
<tr>
<td>.  .  .  .  .  .  .  .</td>
<td>1  0  1</td>
<td>1  0  0  0  1</td>
<td></td>
</tr>
<tr>
<td>.  .  .  .  .  .  .  .</td>
<td>1  1  0</td>
<td>1  0  0  0  1</td>
<td></td>
</tr>
<tr>
<td>.  .  .  .  .  .  .  .</td>
<td>1  1  1</td>
<td>0  0  0  0  0</td>
<td></td>
</tr>
<tr>
<td>0  0  0  0  x  1  1  1</td>
<td>0  0  0  0  0  0</td>
<td>x  x  x  1  0  0  0  1</td>
<td>Pattern 8</td>
</tr>
<tr>
<td>.  .  .  .  .  .  .  .</td>
<td>0  0  1</td>
<td>1  0  0  0  1</td>
<td></td>
</tr>
<tr>
<td>.  .  .  .  .  .  .  .</td>
<td>0  1  0</td>
<td>1  0  0  0  1</td>
<td></td>
</tr>
<tr>
<td>.  .  .  .  .  .  .  .</td>
<td>0  1  1</td>
<td>1  1  1  1  1</td>
<td></td>
</tr>
<tr>
<td>.  .  .  .  .  .  .  .</td>
<td>1  0  0</td>
<td>1  0  0  0  1</td>
<td></td>
</tr>
<tr>
<td>.  .  .  .  .  .  .  .</td>
<td>1  0  1</td>
<td>1  0  0  0  1</td>
<td></td>
</tr>
<tr>
<td>.  .  .  .  .  .  .  .</td>
<td>1  1  0</td>
<td>1  0  0  0  1</td>
<td></td>
</tr>
<tr>
<td>.  .  .  .  .  .  .  .</td>
<td>1  1  1</td>
<td>0  0  0  0  0</td>
<td></td>
</tr>
</tbody>
</table>
INSTRUCTION DESCRIPTION

Outline
To overcome the speed difference between internal clock of S6A0069 and MPU clock, S6A0069 performs internal operation by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus. (refer to Table 5 ) Instruction can be divided largely four kinds,

1) S6A0069 function set instructions ( set display methods, set data length, etc.)
2) Address set instructions to internal RAM
3) Data transfer instructions with internal RAM
4) Others.

The address of internal RAM is automatically increased or decreased by 1.

NOTE: During internal operation, Busy Flag (DB7) is read High. Busy Flag check must precede the next instruction. When an MPU program with checking the Busy Flag (DB7) is made, it must be necessary 1/2 fosc for executing the next instruction by the falling edge of the ‘E’ signal after the Busy Flag (DB7) goes to "LOW".

Contents
1) Clear Display

<table>
<thead>
<tr>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>DB6</th>
<th>DB5</th>
<th>DB4</th>
<th>DB3</th>
<th>DB2</th>
<th>DB1</th>
<th>DB0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Clear all the display data by writing ”20H” (space code) to all DDRAM address, and set DDRAM address to ”00H” into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

2) Return Home

<table>
<thead>
<tr>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>DB6</th>
<th>DB5</th>
<th>DB4</th>
<th>DB3</th>
<th>DB2</th>
<th>DB1</th>
<th>DB0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>-</td>
</tr>
</tbody>
</table>

Return Home is cursor return home instruction. Set DDRAM address to ”00H” into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.
3) Entry Mode Set

```
RS  R/W  DB7  DB6  DB5  DB4  DB3  DB2  DB1  DB0
0   0   0   0   0   0   0   1   I/D  SH
```

Set the moving direction of cursor and display.

**I/D : Increment / decrement of DDRAM address (cursor or blink)**

When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM operates the same as DDRAM, when read from or write to CGRAM.

**SH: Shift of entire display**

When DDRAM read (CGRAM read/write) operation or SH = "Low", shift of entire display is not performed. If SH = "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "1" : shift left, I/D = "0" : shift right).

4) Display ON / OFF Control

```
RS  R/W  DB7  DB6  DB5  DB4  DB3  DB2  DB1  DB0
0   0   0   0   0   0   1   D   C   B
```

Control display/cursor/blink ON/OFF 1 bit register.

**D : Display ON/OFF Control Bit**

When D = "High", entire display is turned on.
When D = "Low", display is turned off, but display data is remained in DDRAM.

**C : Cursor ON/OFF Control Bit**

When C = "High", cursor is turned on.
When C = "Low", cursor is disappeared in current display, but I/D register remains its data.

**B : Cursor Blink ON/OFF Control Bit**

When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position.
When B = "Low", blink is off.

5) Cursor or Display Shift

```
RS  R/W  DB7  DB6  DB5  DB4  DB3  DB2  DB1  DB0
0   0   0   0   0   1   S/C  R/L  -   -
```

Shifting of right/left cursor position or display without writing or reading of display data. This instruction is used to correct or search display data (Refer to table 6). During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line. Note that display shift is performed simultaneously in all the lines. When displayed data is shifted repeatedly, each line is shifted individually. When display shift is performed, the contents of the address counter are not changed.
Table 6. Shift Patterns According to S/C and R/L Bits

<table>
<thead>
<tr>
<th>S/C</th>
<th>R/L</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Shift cursor to the left, AC is decreased by 1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Shift cursor to the right, AC is increased by 1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Shift all the display to the left, cursor moves according to the display</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Shift all the display to the right, cursor moves according to the display</td>
</tr>
</tbody>
</table>

6) Function Set

RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 1 DL N F - -

DL : Interface Data Length Control Bit
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode. When 4-bit bus mode, it needs to transfer 4-bit data by two times.

N : Display Line Number Control Bit
When N = "Low", it means 1-line display mode.
When N = "High", 2-line display mode is set.

F : Display Font Type Control Bit
When F = "Low", it means 5 × 8 dots format display mode
When F = "High", 5 × 11 dots format display mode.

7) Set CGRAM Address

RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 1 AC5 AC4 AC3 AC2 AC1 AC0

Set CGRAM address to AC. This instruction makes CGRAM data available from MPU.

8) Set DDRAM Address

RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 1 AC6 AC5 AC4 AC3 AC2 AC1 AC0

Set DDRAM address to AC. This instruction makes DDRAM data available from MPU. When 1-line display mode (N = 0), DDRAM address is from "00H" to "4FH". In 2-line display mode (N = 1), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

9) Read Busy Flag & Address

RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 1 BF AC6 AC5 AC4 AC3 AC2 AC1 AC0

This instruction shows whether S6A0069 is in internal operation or not. If the resultant BF is High, it means the internal operation is in progress and you have to wait until BF to be Low, and then the next instruction can be performed. In this instruction you can read also the value of address counter.
10) Write Data to RAM

<table>
<thead>
<tr>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>DB6</th>
<th>DB5</th>
<th>DB4</th>
<th>DB3</th>
<th>DB2</th>
<th>DB1</th>
<th>DB0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
</tr>
</tbody>
</table>

Write binary 8-bit data to DDRAM/CGRAM. The selection of RAM from DDRAM, CGRAM, is set by the previous address set instruction (DDRAM address set, CGRAM address set). RAM set instruction can also determine the AC direction to RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

11) Read Data from RAM

<table>
<thead>
<tr>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>DB6</th>
<th>DB5</th>
<th>DB4</th>
<th>DB3</th>
<th>DB2</th>
<th>DB1</th>
<th>DB0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
</tr>
</tbody>
</table>

Read binary 8-bit data from DDRAM/CGRAM. The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data. In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction: it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

**NOTE:** In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.
## Table 7. Instruction Table

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Instruction Code</th>
<th>Description</th>
<th>Execution time (fsoc=270kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clear Display</td>
<td>RS 0 R/W 0 DB7 0 DB6 0 DB5 0 DB4 0 DB3 0 DB2 0 DB1 0 1</td>
<td>Write &quot;20H&quot; to DDRAM and set DDRAM address to &quot;00H&quot; from AC.</td>
<td>1.53ms</td>
</tr>
<tr>
<td>Return Home</td>
<td>RS 0 R/W 0 DB7 0 DB6 0 DB5 0 DB4 0 DB3 0 DB2 0 DB1 0 1 X</td>
<td>Set DDRAM address to &quot;00H&quot; from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.</td>
<td>1.53ms</td>
</tr>
<tr>
<td>Entry Mode Set</td>
<td>RS 0 R/W 0 DB7 0 DB6 0 DB5 0 DB4 0 DB3 0 DB2 0 DB1 0 1 I/D SH</td>
<td>Assign cursor moving direction and make shift of entire display enable.</td>
<td>39µs</td>
</tr>
<tr>
<td>Display ON/OFF Control</td>
<td>RS 0 R/W 0 DB7 0 DB6 0 DB5 0 DB4 0 DB3 0 DB2 0 DB1 0 1 D C B</td>
<td>Set display(D), cursor(C), and blinking of cursor(B) on/off control bit.</td>
<td>39µs</td>
</tr>
<tr>
<td>Cursor or Display Shift</td>
<td>RS 0 R/W 0 DB7 0 DB6 0 DB5 0 DB4 0 DB3 0 DB2 0 DB1 0 1 S/C R/L X X</td>
<td>Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.</td>
<td>39µs</td>
</tr>
<tr>
<td>Function Set</td>
<td>RS 0 R/W 0 DB7 0 DB6 0 DB5 0 DB4 0 DB3 0 DB2 0 DB1 0 1 DL N F X X</td>
<td>Set interface data length (DL : 4-bit/8-bit), numbers of display line (N : 1-line/2-line), display font type(F : 5 X 8 dots/ 5 X 11 dots)</td>
<td>39µs</td>
</tr>
<tr>
<td>Set CGRAM Address</td>
<td>RS 0 R/W 0 DB7 0 DB6 0 DB5 0 DB4 0 DB3 0 DB2 0 DB1 0 1 AC5 AC4 AC3 AC2 AC1 AC0</td>
<td>Set CGRAM address in address counter.</td>
<td>39µs</td>
</tr>
<tr>
<td>Set DDRAM Address</td>
<td>RS 0 R/W 0 DB7 0 DB6 0 DB5 0 DB4 0 DB3 0 DB2 0 DB1 0 1 AC6 AC5 AC4 AC3 AC2 AC1 AC0</td>
<td>Set DDRAM address in address counter.</td>
<td>39µs</td>
</tr>
<tr>
<td>Read Busy Flag and Address</td>
<td>RS 0 R/W 0 DB7 0 DB6 0 DB5 0 DB4 0 DB3 0 DB2 0 DB1 0 1 BF AC6 AC5 AC4 AC3 AC2 AC1 AC0</td>
<td>Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.</td>
<td>0µs</td>
</tr>
<tr>
<td>Write Data to RAM</td>
<td>RS 0 R/W 0 DB7 0 DB6 0 DB5 0 DB4 0 DB3 0 DB2 0 DB1 0 1 D7 D6 D5 D4 D3 D2 D1 D0</td>
<td>Write data into internal RAM (DDRAM/CGRAM).</td>
<td>43µs</td>
</tr>
<tr>
<td>Read Data from RAM</td>
<td>RS 0 R/W 0 DB7 0 DB6 0 DB5 0 DB4 0 DB3 0 DB2 0 DB1 0 1 D7 D6 D5 D4 D3 D2 D1 D0</td>
<td>Read data from internal RAM (DDRAM/CGRAM).</td>
<td>43µs</td>
</tr>
</tbody>
</table>

**NOTE:** When an MPU program with checking the Busy Flag (DB7) is made, it must be necessary 1/2 fosc is necessary for executing the next instruction by the falling edge of the 'E' signal after the Busy Flag (DB7) goes to "LOW".
INTERFACE WITH MPU

1) Interface with 8-bit MPU

When interfacing data length is 8-bit, transfer is performed at a time through 8 ports, from DB0 to DB7. Example of timing sequence is shown below.

![Figure 4. Example of 8-bit Bus Mode Timing Diagram](image-url)
2) Interface with 4-bit MPU

When interfacing data length is 4-bit, only 4 ports, from DB4 to DB7, are used as data bus. At first higher 4-bit (in case of 8-bit bus mode, the contents of DB4 - DB7) are transferred, and then lower 4-bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred. So transfer is performed by two times. Busy Flag outputs "High" after the second transfer are ended. Example of timing sequence is shown below.

Figure 5. Example of 4-bit Bus Mode Timing Diagram
APPLICATION INFORMATION ACCORDING TO LCD PANEL

1) LCD Panel: 8 Character × 1-line Character Format; 5 × 7 dots + 1-cursor line (1/4 Bias, 1/8 Duty)

2) LCD Panel: 8 Character × 1-line Character Format; 5 × 10 dots + 1 cursor line (1/4 Bias, 1/11 Duty)
3) LCD Panel: 8 Character × 2-line Character Format; 5 × 7 dots + 1-cursor line (1/5 Bias, 1/16 Duty)
4) LCD Panel: 16 Character ×1-line Character Format; 5×7 dots + 1-cursor line (1/5 Bias, 1/16 Duty)
5) LCD Panel: 4 Character × 2-line Character Format; 5 × 7 dots + 1-cursor line (1/4 Bias, 1/8 Duty)
6) APPLICATION CIRCUIT

NOTE: When S6A0065 is externally connected to the S6A0069, you can increase the number of display digits up to 80 characteristics.
BIAS VOLTAGE DIVIDE CIRCUIT

1) 1/4 bias, 1/8 or 1/11 duty

2) 1/5 bias, 1/16 duty
INITIALIZING

When the power is turned on, S6A0069 is initialized automatically by power on reset circuit. During the initialization, the following instructions are executed, and BF(Busy Flag) is kept "High"(busy state) to the end of initialization.

(1) Display Clear instruction: Write "20H" to all DDRAM
(2) Set Functions instruction
   \[ DL = 1 : 8\text{-bit bus mode} \]
   \[ N = 1 : 2\text{-line display mode} \]
   \[ F = 0 : 5 \times 8 \text{ font type} \]
(3) Control Display ON/OFF instruction
   \[ D = 0 : \text{Display OFF} \]
   \[ C = 0 : \text{Cursor OFF} \]
   \[ B = 0 : \text{Blink OFF} \]
(4) Set Entry Mode instruction
   \[ I/D = 1 : \text{Increment by 1} \]
   \[ SH = 0 : \text{No entire display shift} \]

FRAME FREQUENCY

Programmable Driving Method by the same font mask option: Display waveform A-Type, B-Type

1) 1/8 Duty Cycle

A) A-Type Waveform

B) B-Type Waveform

Line selection period = 400 clocks
One Frame = 400 x 8 x 3.7μs = 11850 μs = 11.9 ms (1 clock = 3.7 μs, fosc = 270kHz)
Frame frequency = 1 / 11.9ms = 84.3Hz
2) 1/11 duty cycle

A) A-type Waveform

B) B-type Waveform

Line selection period = 400 clocks
One Frame = 400 × 11 × 3.7μs = 16300μs = 16.3ms (1 clock = 3.7μs, fosc = 270kHz)
Frame frequency = 1 / 16.3 ms = 61.4 Hz
3) 1/16 duty cycle

A) A-type Waveform

B) B-type Waveform

Line selection period = 200 clocks
One Frame = 200 x 16 x 3.7\mu s = 11850 \mu s = 11.9 ms (1 clock = 3.7\mu s, fosc = 270kHz)
Frame frequency = 1 / 11.9ms = 84.3Hz
INITIALIZING BY INSTRUCTION

1) 8-bit Interface Mode (Condition: fosc = 270kHz)

- Power On
  - Wait for more than 30ms after VDD rises to 4.5 V.
  - Wait for more than 40ms after VDD rises to 2.7 V.

- Function Set
  - N 0 1-line mode
    1 2-line mode
  - F 0 Display OFF
    1 Display ON
  - D 0 Display OFF
    1 Display ON
  - C 0 Cursor OFF
    1 Cursor ON
  - B 0 Blink OFF
    1 Blink ON

- Display ON/OFF Control
  - Wait for more than 3µs

- Display Clear
  - Wait for more than 1.5ms

- Entry Mode Set
  - I/D 0 Decrement mode
    1 Increment mode
  - SH 0 Entire shift off
    1 Entire shift on

- Initialization End
2) 4-bit Interface Mode (Condition: fosc = 270kHz)

- **Power On**: Wait for more than 30ms after \( V_{DD} \) rises to 4.5 V. Wait for more than 40ms after \( V_{DD} \) rises to 2.7 V.

### Function Set

<table>
<thead>
<tr>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>DB6</th>
<th>DB5</th>
<th>DB4</th>
<th>DB3</th>
<th>DB2</th>
<th>DB1</th>
<th>DB0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>DL</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>N</td>
<td>0</td>
<td>F</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

- **Wait for more than 39s**

### Display ON/OFF Control

<table>
<thead>
<tr>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>DB6</th>
<th>DB5</th>
<th>DB4</th>
<th>DB3</th>
<th>DB2</th>
<th>DB1</th>
<th>DB0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>D</td>
<td>C</td>
</tr>
</tbody>
</table>

- **Wait for more than 39s**

### Display Clear

<table>
<thead>
<tr>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>DB6</th>
<th>DB5</th>
<th>DB4</th>
<th>DB3</th>
<th>DB2</th>
<th>DB1</th>
<th>DB0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>X</td>
</tr>
</tbody>
</table>

- **Wait for more than 1.53ms**

### Entry Mode Set

<table>
<thead>
<tr>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>DB6</th>
<th>DB5</th>
<th>DB4</th>
<th>DB3</th>
<th>DB2</th>
<th>DB1</th>
<th>DB0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>I/D</td>
<td>SH</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

- **Initialization End**

### Other Settings

- **D/L**: 0 4-bit mode  |
  1 8-bit mode  |
- **N**: 0 1-line mode  |
  1 2-line mode  |
- **F**: 0 Display off  |
  1 Display on  |
- **D**: 0 Display off  |
  1 Display on  |
- **C**: 0 Cursor off  |
  1 Cursor on  |
- **B**: 0 Blink off  |
  1 Blink on  |
- **I/D**: 0 Decrement mode  |
  1 Increment mode  |
- **SH**: 0 Entire shift off  |
  1 Entire shift on  |

Wait for more than 30ms after \( V_{DD} \) rises to 4.5 V. Wait for more than 40ms after \( V_{DD} \) rises to 2.7 V.
### MAXIMUM ABSOLUTE LIMIT

**Maximum Absolute Power Ratings**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Unit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Voltage</td>
<td>$V_{DD}$</td>
<td>V</td>
<td>-0.3 to +7.0</td>
</tr>
<tr>
<td>LCD Drive Voltage</td>
<td>$V_{LCD}$</td>
<td>V</td>
<td>$V_{DD}$-15.0 to $V_{DD}$+0.3</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>$V_{IN}$</td>
<td>V</td>
<td>-0.3 to $V_{DD}$+ 0.3</td>
</tr>
</tbody>
</table>

Voltage greater than above may damage the circuit ($V_{DD} ≥ V_1 ≥ V_2 ≥ V_3 ≥ V_4 ≥ V_5$)

**Temperature Characteristics**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Unit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Temperature</td>
<td>$T_{OPR}$</td>
<td>°C</td>
<td>-30 to +85</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>$T_{STG}$</td>
<td>°C</td>
<td>-55 to +125</td>
</tr>
</tbody>
</table>
## ELECTRICAL CHARACTERISTICS

### DC Characteristics ($V_{DD} = 4.5V$ to $5.5V$, $Ta = -30$ to $+85^\circ C$)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Voltage</td>
<td>$V_{DD}$</td>
<td>-</td>
<td>4.5</td>
<td>-</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Operating Current</td>
<td>$I_{DD}$</td>
<td>Internal oscillation or</td>
<td>-</td>
<td>0.35</td>
<td>0.6</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>external clock ($V_{DD} = 5.0V$,</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{osc} = 270kHz$)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage (1)</td>
<td>$V_{IH1}$</td>
<td>-</td>
<td>2.2</td>
<td>-</td>
<td>$V_{DD}$</td>
<td>V</td>
</tr>
<tr>
<td>(except OSC1)</td>
<td>$V_{IL1}$</td>
<td>-</td>
<td>-0.3</td>
<td>-</td>
<td>0.6</td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage (2)</td>
<td>$V_{IH2}$</td>
<td>$V_{DD}$-1.0</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(OSC1)</td>
<td>$V_{IL2}$</td>
<td>-</td>
<td>-0.2</td>
<td>-</td>
<td>1.0</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage (1)</td>
<td>$V_{OH1}$</td>
<td>$I_{OH} = -0.205mA$</td>
<td>2.4</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>(DB0 to DB7)</td>
<td>$V_{OL1}$</td>
<td>$I_{OL} = 1.2mA$</td>
<td>-</td>
<td></td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage (2)</td>
<td>$V_{OH2}$</td>
<td>$I_{O} = -40\mu A$</td>
<td>0.9$V_{DD}$</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>(except DB0 to DB7)</td>
<td>$V_{OL2}$</td>
<td>$I_{O} = 40\mu A$</td>
<td>-</td>
<td></td>
<td>0.1$V_{DD}$</td>
<td>V</td>
</tr>
<tr>
<td>Voltage Drop</td>
<td>$V_{d_{COM}}$</td>
<td>$I_{O} = \pm 0.1mA$</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{d_{SEG}}$</td>
<td>$V_{IN} = 0V$ to $V_{DD}$</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td>Input Low Current</td>
<td>$I_{IL}$</td>
<td>$V_{IN} = 0V$, $V_{DD} = 5V$ (pull</td>
<td>-50</td>
<td>-125</td>
<td>-250</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>up)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal Clock (external Rf)</td>
<td>$f_{OSC1}$</td>
<td>$Rf = 91k\Omega \pm 2%$ ($V_{DD} = 5V$)</td>
<td>190</td>
<td>270</td>
<td>350</td>
<td>kHz</td>
</tr>
<tr>
<td>External Clock</td>
<td>$f_{OSC}$</td>
<td>-</td>
<td>125</td>
<td>270</td>
<td>350</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td>duty</td>
<td>-</td>
<td>45</td>
<td>50</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>$t_{R}$, $t_{F}$</td>
<td>-</td>
<td>-</td>
<td></td>
<td>0.2</td>
<td>µA</td>
</tr>
<tr>
<td>LCD Driving Voltage</td>
<td>$V_{LCD}$</td>
<td>$V_{DD}$-$V_{5}$ (1/5, 1/4 bias)</td>
<td>3.0</td>
<td>-</td>
<td>13.0</td>
<td>V</td>
</tr>
</tbody>
</table>
### DC Characteristics ($V_{DD} = 2.7V$ to $4.5V$, $Ta = -30$ to $+85°C$)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Voltage</td>
<td>$V_{DD}$</td>
<td>-</td>
<td>2.7</td>
<td>-</td>
<td>4.5</td>
<td>V</td>
</tr>
<tr>
<td>Operating Current</td>
<td>$I_{DD}$</td>
<td>$V_{DD} = 3.0V$, osc = 270kHz</td>
<td>-</td>
<td>0.15</td>
<td>0.3</td>
<td>mA</td>
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<tr>
<td>Input Voltage (1)</td>
<td>$V_{IH1}$</td>
<td>-</td>
<td>0.7</td>
<td>$V_{DD}$</td>
<td>-</td>
<td>$V_{DD}$</td>
</tr>
<tr>
<td>(except OSC1)</td>
<td>$V_{IL1}$</td>
<td>-</td>
<td>-</td>
<td>-0.3</td>
<td>-</td>
<td>0.55</td>
</tr>
<tr>
<td>Input Voltage (2)</td>
<td>$V_{IH2}$</td>
<td>-</td>
<td>0.7</td>
<td>$V_{DD}$</td>
<td>-</td>
<td>$V_{DD}$</td>
</tr>
<tr>
<td>(OSC1)</td>
<td>$V_{IL2}$</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>0.2</td>
<td>$V_{DD}$</td>
</tr>
<tr>
<td>Output Voltage (1)</td>
<td>$V_{OH1}$</td>
<td>$I_{OH} = -0.1mA$</td>
<td>0.75</td>
<td>$V_{DD}$</td>
<td>-</td>
<td>-</td>
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<tr>
<td>(DB0 to DB7)</td>
<td>$V_{OL1}$</td>
<td>$I_{OL} = 0.1mA$</td>
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<td>0.2</td>
<td>$V_{DD}$</td>
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<tr>
<td>Output Voltage (2)</td>
<td>$V_{OH2}$</td>
<td>$I_{O} = -40\mu A$</td>
<td>0.8</td>
<td>$V_{DD}$</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>(except DB0 to DB7)</td>
<td>$V_{OL2}$</td>
<td>$I_{O} = 40\mu A$</td>
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<td>0.2</td>
<td>$V_{DD}$</td>
</tr>
<tr>
<td>Voltage Drop</td>
<td>$V_{dCOM}$</td>
<td>$I_{O} = \pm 0.1mA$</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{dSEG}$</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>V</td>
</tr>
<tr>
<td>Input Leakage Current</td>
<td>$I_{LKG}$</td>
<td>$V_{IN} = 0V - V_{DD}$</td>
<td>-1</td>
<td>-</td>
<td>1</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>Input Low Current</td>
<td>$I_{IL}$</td>
<td>$V_{IN} = 0V$, $V_{DD} = 3V$ (pull up)</td>
<td>-10</td>
<td>-50</td>
<td>-120</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>Internal Clock (external</td>
<td>$f_{OSC1}$</td>
<td>$Rf = 75k\Omega \pm 2%$ ($V_{DD} = 3V$)</td>
<td>190</td>
<td>270</td>
<td>350</td>
<td>kHz</td>
</tr>
<tr>
<td>RF)</td>
<td>$f_{OSC2}$</td>
<td>-</td>
<td>125</td>
<td>270</td>
<td>410</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td>duty</td>
<td>-</td>
<td>45</td>
<td>50</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td>External Clock</td>
<td>$t_{R}$, $f_{F}$</td>
<td>-</td>
<td>0.2</td>
<td>-</td>
<td>0.2</td>
<td>$\mu S$</td>
</tr>
<tr>
<td>LCD Driving Voltage</td>
<td>$V_{LCD}$</td>
<td>$V_{DD} \cdot V_{5}$ ($1/5$, $1/4$ bias)</td>
<td>3.0</td>
<td>-</td>
<td>13.0</td>
<td>V</td>
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</tbody>
</table>

**NOTE:** LCD Driving Voltage

<table>
<thead>
<tr>
<th>Power</th>
<th>Duty</th>
<th>1/8, 1/11 Duty</th>
<th>1/16 Duty</th>
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</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>1/4 Bias</td>
<td>1/5 Bias</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>$V_{DD}$</td>
<td>$V_{DD}$</td>
<td></td>
</tr>
<tr>
<td>$V_{1}$</td>
<td>$V_{DD} \cdot V_{LCD}/4$</td>
<td>$V_{DD} \cdot V_{LCD}/5$</td>
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</tr>
<tr>
<td>$V_{2}$</td>
<td>$V_{DD} \cdot V_{LCD}/2$</td>
<td>$V_{DD} \cdot 2V_{LCD}/5$</td>
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</tr>
<tr>
<td>$V_{3}$</td>
<td>$V_{DD} \cdot V_{LCD}/2$</td>
<td>$V_{DD} \cdot 3V_{LCD}/5$</td>
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<tr>
<td>$V_{4}$</td>
<td>$V_{DD} \cdot 3V_{LCD}/4$</td>
<td>$V_{DD} \cdot 4V_{LCD}/5$</td>
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<tr>
<td>$V_{5}$</td>
<td>$V_{DD} \cdot V_{LCD}$</td>
<td>$V_{DD} \cdot V_{LCD}$</td>
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</tr>
</tbody>
</table>
### AC Characteristics

\((V_{DD} = 4.5 \text{ to } 5.5V, \, Ta = -30 \text{ to } +85^\circ C)\)

<table>
<thead>
<tr>
<th>Mode</th>
<th>Characteristics</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write Mode (refer to Figure-6)</td>
<td>E Cycle Time</td>
<td>tc</td>
<td>500</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>E Rise / Fall Time</td>
<td>2tR, tF</td>
<td>-</td>
<td>-</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td></td>
<td>E Pulse Width (High, Low)</td>
<td>tw</td>
<td>230</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td></td>
<td>R/W and RS Setup Time</td>
<td>tsu1</td>
<td>40</td>
<td>-</td>
<td>-</td>
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</tr>
<tr>
<td></td>
<td>R/W and RS Hold Time</td>
<td>tH1</td>
<td>10</td>
<td>-</td>
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<tr>
<td></td>
<td>Data Setup Time</td>
<td>tsu2</td>
<td>80</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Data Hold Time</td>
<td>tH2</td>
<td>10</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>

| Read Mode (refer to Figure-7) | E Cycle Time                     | tc     | 500 | -   | -   | ns   |
|                                | E Rise / Fall Time                | 2tR, tF | -   | -   | 20  |      |
|                                | E Pulse Width (High, Low)         | tw     | 230 | -   | -   |      |
|                                | R/W and RS Setup Time             | tsu    | 40  | -   | -   |      |
|                                | R/W and RS Hold Time              | tH    | 10  | -   | -   |      |
|                                | Data Output Delay Time            | tD     | -   | -   | 120 |      |
|                                | Data Hold Time                    | tDH    | 5   | -   | -   |      |

\((V_{DD} = 2.7 \text{ to } 4.5V, \, Ta = -30 \text{ to } +85^\circ C)\)

<table>
<thead>
<tr>
<th>Mode</th>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write Mode (refer to Figure-6)</td>
<td>E Cycle Time</td>
<td>tc</td>
<td>1000</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>E Rise / Fall Time</td>
<td>2tR, tF</td>
<td>-</td>
<td>-</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td></td>
<td>E Pulse Width (High, Low)</td>
<td>tw</td>
<td>450</td>
<td>-</td>
<td>-</td>
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</tr>
<tr>
<td></td>
<td>R/W and RS Setup Time</td>
<td>tsu1</td>
<td>60</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td></td>
<td>R/W and RS Hold Time</td>
<td>tH1</td>
<td>20</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Data Setup Time</td>
<td>tsu2</td>
<td>195</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Data Hold Time</td>
<td>tH2</td>
<td>10</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>

| Read Mode (refer to Figure-7) | E Cycle Time                     | tc     | 1000| -   | -   | ns   |
|                                | E Rise / Fall Time                | 2tR, tF | -   | -   | 25  |      |
|                                | E Pulse Width (High, Low)         | tw     | 450 | -   | -   |      |
|                                | R/W and RS Setup Time             | tsu    | 60  | -   | -   |      |
|                                | R/W and RS Hold Time              | tH    | 20  | -   | -   |      |
|                                | Data Output Delay Time            | tD     | -   | -   | 360 |      |
|                                | Data Hold Time                    | tDH    | 5   | -   | -   |      |
(V_{DD} = 2.7 to 4.5V, Ta = -30 to +85°C)

<table>
<thead>
<tr>
<th>Mode</th>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interface Mode with Extension Driver (refer to Figure-8)</td>
<td>Clock Pulse Width (High, Low)</td>
<td>tw</td>
<td>800</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Clock Rise / Fall Time</td>
<td>t_R, t_F</td>
<td>-</td>
<td>-</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>Clock Setup Time</td>
<td>tsu1</td>
<td>500</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Data Setup Time</td>
<td>tsu2</td>
<td>300</td>
<td>-</td>
<td>-</td>
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</tr>
<tr>
<td></td>
<td>Data Hold Time</td>
<td>t_{DH}</td>
<td>300</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td></td>
<td>M Delay Time</td>
<td>t_{DM}</td>
<td>-1000</td>
<td>-</td>
<td>1000</td>
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</tr>
</tbody>
</table>

Figure 6. Write Mode Timing Diagram

Figure 7. Read Mode Timing Diagram
Figure 8. Interface Mode with Extension Driver Timing Diagram
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