Power Supply Transient Signal Integration Circuit

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Abstract

Discussed is a circuit which measures and analyses power supply transients as defined in the test technique, Transient Signal Analysis (TSA). This circuit can replace the bench-top instrumentation and offline signal processing software used in previous work. The circuit accepts voltage transients as analog inputs from the Device-Under-Test (DUT), performs integration and outputs an analog value to the tester. The tester compares the output value to a predetermined threshold as a means of determining the pass/fail status of the DUT. This circuit is designed to simplify the hardware requirements of TSA.

1.0 Introduction

Transient Signal Analysis (TSA) is a parametric approach to testing digital integrated circuits [1][2]. Defect detection in TSA is accomplished by analyzing the power supply transient signals measured at multiple supply pads on the DUT. It is found that defects can be observed as excessive signal variations coupled to the power rails. Unfortunately, fabrication process variations also introduce significant signal variations in the supply pad signals. To distinguish between these sources (i.e. real failure vs. false reject), TSA defines a screening procedure based on cross-correlating a set of voltage transient measurements collected at multiple supply pads, and comparing that data to a reference profile pre-characterized using a set of "good" devices. A reasonable reference profile can be iteratively constructed using the procedure outlined in [9].

The profile is a set of regression fits of pairwise supply pad measurements that define the signal characteristics of a good device. In this way the profile compensates for signal variations due to process variations. Thus, assuming that process variation is uniform across the die and more disjoint, or pronounced, between die then within die, defect-free test device data should track the regression fit.

The TSA procedure demonstrated in previous works was carried out using digital signal processing (DSP) routines and benchtop oscilloscopes. The hardware circuit proposed in this paper, called the Supply Transient Integration Circuit, or STIC, is designed to replace a portion of that "development system."

This work was done while Chintan Patel was an employee at Agilent Technologies.

The STIC performs measurement and signal processing on time domain signals as defined by the TSA method. It accepts two power supply transient signals as inputs: one from the Device-Under-Test (DUT) and a second from a reference device (which can be the same device or a known defect-free reference device) or a tester channel. From these, it computes a difference waveform, performs a special integration operation and delivers an analog signal that represents the result to the tester. The functions are carried out in the STIC using high frequency operational amplifiers.

The tester compares the STIC output to a limit derived from a pre-characterized reference profile and either passes or fails the DUT. If the DUT's value is within tolerance, the STIC is reset by the tester and the procedure is repeated with the next test sequence. In order to be acceptable at a tester interface, the current STIC is designed to operate at 300MHz.

The functional requirements of the STIC are defined by the TSA procedure, which are described following the survey of related work given in Section 2.0. Section 4.0 describes the design details of the STIC. Section 5.0 presents simulation results that validate its operation. Section 6.0, presents conclusions and areas for further investigation.

2.0 Background

I_{DDQ} is used extensively to detect defects. Much work has been done in developing on-chip as well as on-board solutions for making I_{DDQ} measurements. However, the effectiveness of I_{DDQ} testing in deep-submicron technologies is reduced due to high background currents and process drift. On the other hand, transient power supply testing (V_{DDT}) techniques, are insensitive to background leakage and may be able to augment the existing tests. Several proposed methods are described in [1],[2],[13]-[17]. To use any such technique in production requires a means of making the transient measurements defined by the respective algorithms with minimum overhead. This has been investigated in [4],[6]-[8],[10]-[12]. Most of these built-in monitors perform only a specific

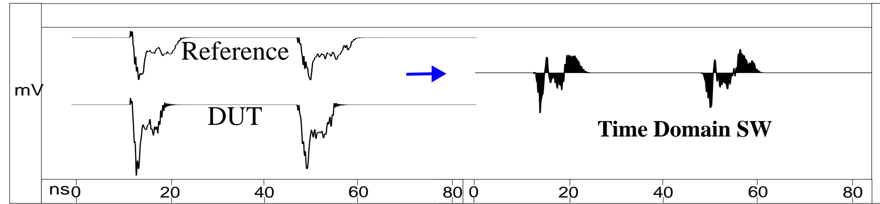


Figure 1. Time Domain Signature Waveforms.

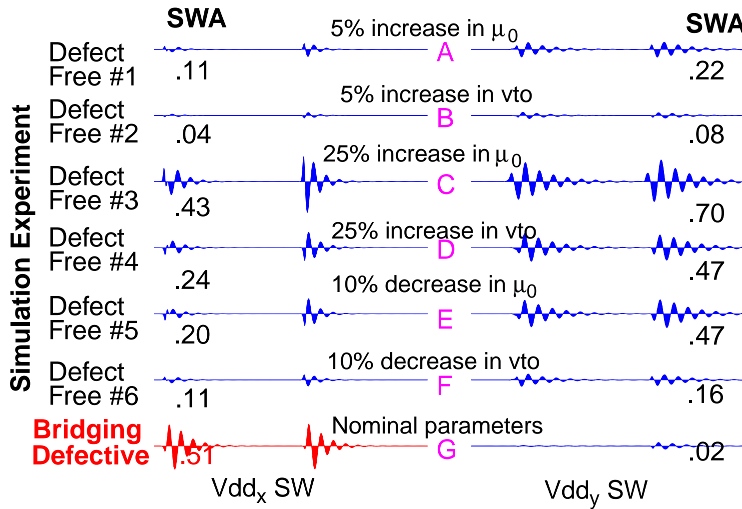


Figure 2. Vdd_x and Vdd_y Signature Waveforms from 7 simulation runs.

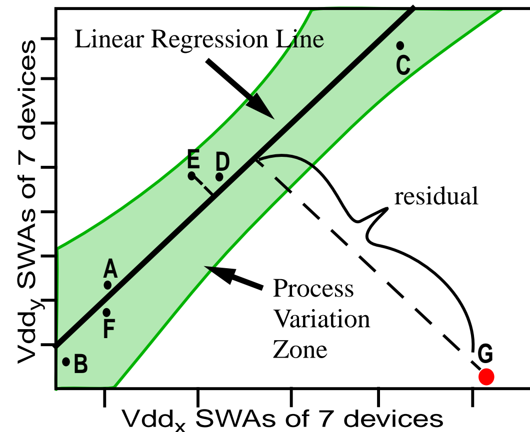


Figure 3. Scatter plot, Regression line and confidence bands for data in figure2.

measurement as required by that particular testing technique. Also, as the amount of signal processing required in many of these techniques is marginal, the area overhead of integrating the monitor on chip is relatively small. However the analog components of these monitors must be robust to process variations affecting the digital logic under test. Moreover the designs themselves must be self-calibrating to these variations. One way to deal with the latter issue is to put the monitor on the load board or the probe card rather than on-chip. However, apart from size and manufacturing floor issues, the main issue in this approach is dealing with noise and other stray interference effects which can affect signal integrity and introduce measurement errors. Thus, any reasonable attempt must consider and compensate for them.

3.0 TSA Algorithm to be Implemented

The STIC implements the TSA algorithm in processing sampled voltage transients. TSA can be applied to the time or frequency domain representation of the transients. In this paper, we focus on the processing of the time domain signals. In TSA, the cross-correlation referred to in section 1.0 is actually performed on a set of area values derived from "difference waveforms". A difference waveform is computed by subtracting the DUT's transient from a reference transient. In this way, only the relative change in the DUT's transient response with respect to the reference is considered in the pass/fail decision process. The difference operation is the strategy used to reduce measurement noise and stray interference, e.g. EMI, that is common in all DUT measurements.

Figure 1 shows two time domain waveforms (left) and their difference waveform shaded to a zero baseline (right). The shaded difference waveform is referred to as a signature waveform (SW). The absolute area, given by the shaded region under the SW is used as input to the cross-correlation method. This area is referred to as a Signature Waveform Area or SWA.

The cross-correlation method is based on linear regression analysis, as illustrated in Figures 2 and 3 using a set of simulation-generated SWs. Figure 2 shows two columns of SWs from two supply pads (Vdd_x and Vdd_y) of a test device. The pairs of SWs in the top six rows correspond to simulation experiments in which transistor mobilities and threshold voltages (μ_0 and vto), are varied globally from the nominal value by the indicated percentage. The pair of SWs in the last row are from a simulation of a bridging defective circuit model. The model used in this "faulted"

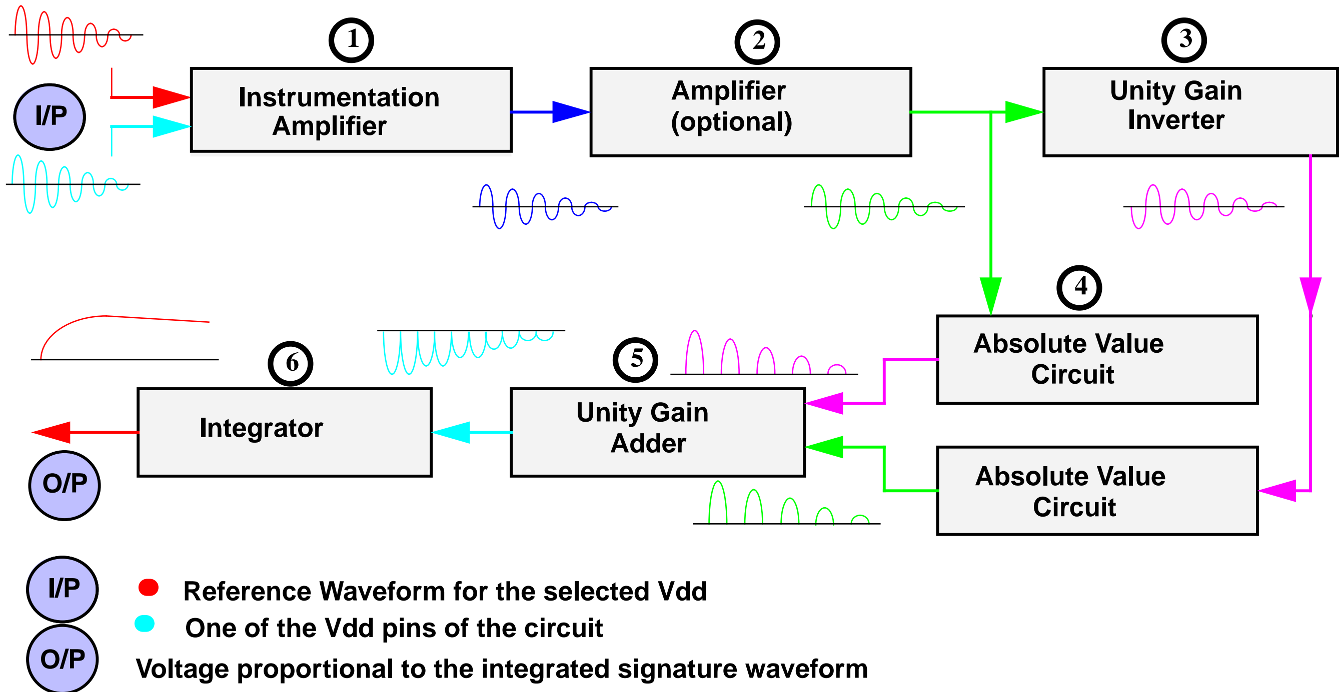


Figure 4. Block Diagram of the Supply Transient Integrator Circuit (STIC).

simulation is identical to the model used in the reference except for the presence of the defect.

Figure 3 illustrates the high correlation in the SWs of the defect-free device process runs (pairs A through F). In this scatterplot, the SWAs from Vdd_x are plotted against the corresponding SWAs from Vdd_y. The linear tracking of the data points given by these pairing is illustrated by the regression line. The Process Variation Zone (PVZ), delineated by 3σ confidence limits, defines the defect-free device region, and accounts for measurement noise and intra-device process variation effects. In contrast, the defective device data point (labeled G) is an outlier with respect to the PVZ. The SWAs that represent it capture the uncorrelated regional variation introduced by the defect. In this case, the defect is in close proximity to supply pad Vdd_x. Other experimental results on TSA can be found in reference [2].

4.0 The Supply Transient Integration Circuit

The TSA concept was demonstrated using digitizing oscilloscopes and a fair amount of offline signal processing. The STIC is designed to replace the oscilloscopes and most of the DSP, as a means of making TSA more amenable to the production test floor.

4.1 Overview of the Supply Transient Integrator Circuit (STIC)

The structure of the STIC is shown in Figure 4. Each of the blocks in the figure transform the signals of the previous stage. All of the circuit components are designed using high frequency operational amplifiers. The operational amplifiers must have both high bandwidth and slew rate to sample the transient signals that have important frequency components at or below the digital DUT's operational frequency. The circuit proposed here uses two different type of opamps, one for the instrumentation amplifier, inverter, adder and integrator stages and one for the absolute value stage. The opamps used for the absolute value stage of the circuit must be capable of operating under a single power supply or a reduced negative supply voltage, as discussed below. Both of the opamp models used in the simulation experiments presented in this paper are commercial models from existing vendor parts, one operates using a +/-15V power supply voltage and the other operates using a +/-5V supply or optionally uses a +5V and a reduced or 0V negative supply.

The inputs to the STIC are signals measured from the power supply pads of the DUT, reference device and/or tester channel. The transients are DC biased at the supply voltage. The first stage of the STIC (Instrumentation Amplifier) removes this bias and generates the difference waveform. The difference is optionally amplified in the second stage. The remaining stages of the STIC are designed to perform the special form of integration required by the TSA method. Here the resulting SWAs represent the sum of the areas under the positive portion of the transient waveform plus the absolute value of the area under the negative portion.

The Absolute Value Circuit components of the STIC

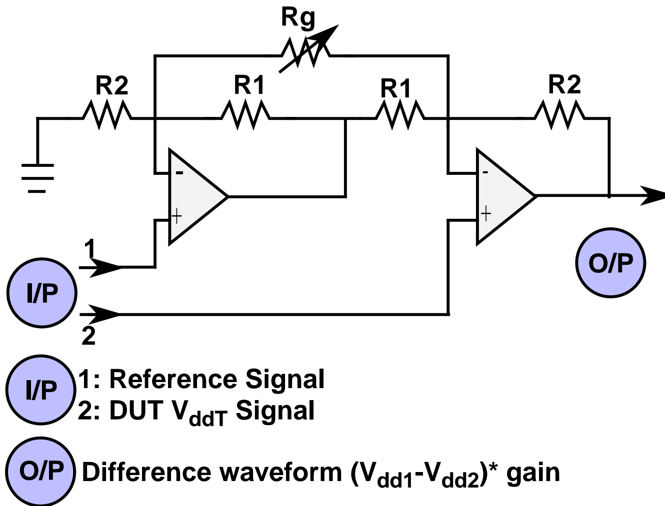


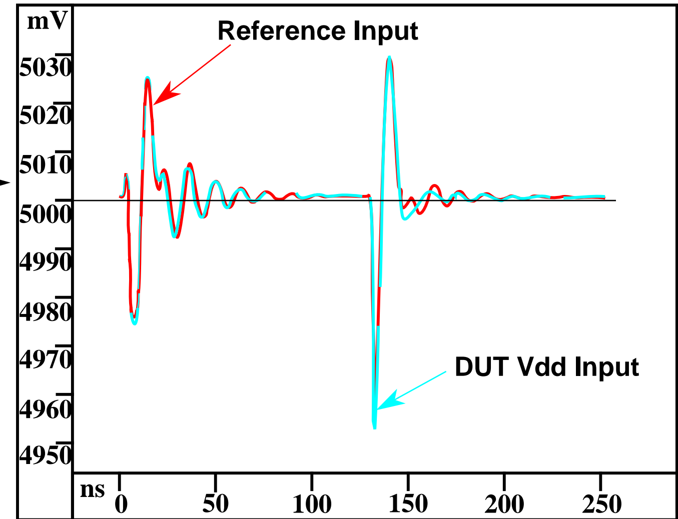
Figure 5. Instrumentation Amplifier (IA) component of the STIC.

(stage 4) are responsible for converting the transient to a unipolar form. The Unity Gain Inverter (stage 3) provides the input to the Absolute Value Circuit responsible for producing the unipolar form of the negative going transients in the original difference waveform. The outputs of the two absolute value circuits are passed on to the adder circuit to generate the full unipolar signal as shown in stage 5. The rectified unipolar signal is then passed to the integrator stage of the STIC in order to compute the total area, as shown by stage 6 in the figure.

4.2 Details of the STIC

The implementation details of each stage of the circuit shown in Figure 4 are discussed in this section. The circuit is designed using a set of discrete components consisting of op-amps, resistors, capacitors and diodes. Spice simulations were used to evaluate the design parameters for each stage of the STIC, using the models provided by the vendors.

The design of the Instrumentation Amplifier is given in Figure 5. This circuit implements a differential amplifier biased to allow amplification of signals up to 100mV. This value is adjustable to account for DUT's which generate more significant variations, but our experience indicates that 100mV is sufficient in current DUT technologies using supply voltages in the range of 3.3-5V. The circuit configuration shown in the figure provides a high degree of accuracy over this voltage range at frequencies up to 300MHz. The circuit can be designed to handle higher frequencies for DUT's with operational frequencies upto 600MHz. We have determined in previous work that frequency components at or below the operation frequency of the DUT are important in our testing procedure but frequencies above the operational frequency are not. Therefore under this definition, the STIC is able to meet the



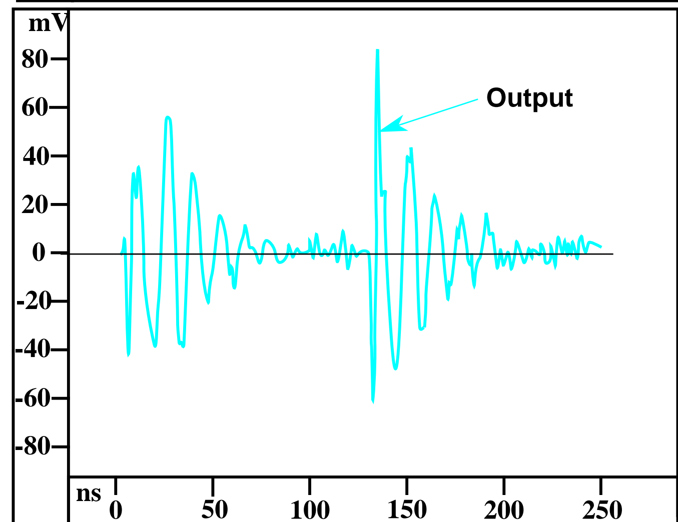


Figure 6. Spice Simulation result curves for the Instrumentation Amplifier component.

testing requirements of many commercial devices.

The left most operational amplifier in Figure 5 acts as an non-inverting amplifier for input signal 1 (reference signal). The output of this op-amp drives the second op-amp, which acts as an inverting amplifier for this input. Variations in the reference signal force the circuit output to track only the difference between the reference waveform and input 2, the DUT's V_{DDT}. The variable resistor Rg is the gain control resistance of the circuit. To ensure linearity, the total gain is set to approximately 10x. Rg provides a means of trading off the operational voltage range and the accuracy of the difference waveform produced. The voltage transfer relationship is given by the following expression:

$$\frac{E_0}{E_I} = -\left(1 + \frac{R_2}{R_1} + 2\frac{R_2}{R_G}\right)$$

where E_0 = Output Voltage OP
E_I = (IP1 - IP2)

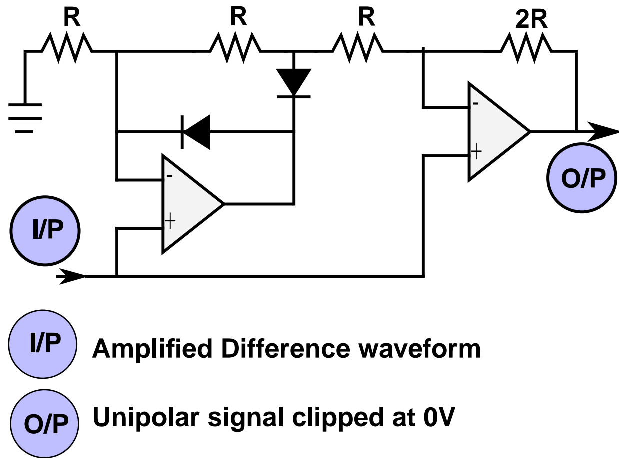


Figure 7. Absolute Value (AV) component of the STIC.

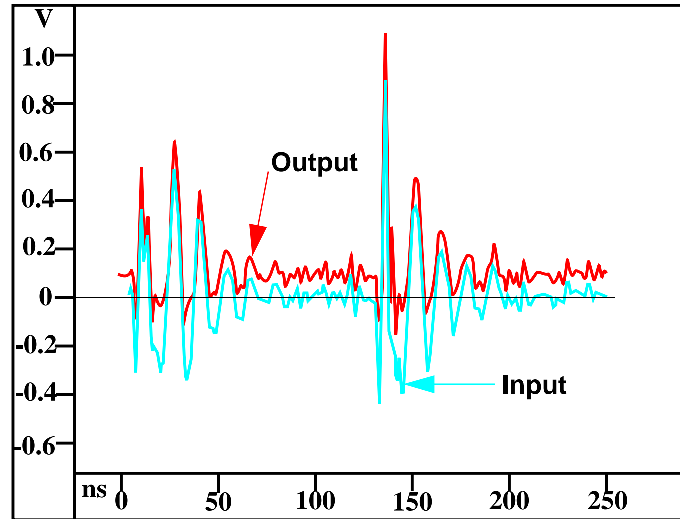


Figure 8. Spice simulation result curves for the AV component.

In this circuit, the common mode rejection error of the two amplifiers tend to cancel but the other errors like offset bias voltage and error due to input bias current are additive. Therefore, special care is taken when biasing this circuit in order to effectively compensate for these inherent limitations of the opamp. Also, any resistor mismatch causes a non-zero common-mode gain that equals the fractional mismatch.

A variety of alternative designs were investigated for this stage of the STIC. It is important to minimize the error in this stage since it is amplified throughout the remaining stages and thus degrades the signal-to-noise ratio. In most cases the difference between the reference waveform and the test waveform is less than 100mV thus imposing further restrictions on the error tolerance of this stage. This stage of the circuit is the most difficult to design. It requires fine tuning since it is dependent to some degree on the DUT's transient characteristics. In particular, the frequency range and average amplitude of the transient must be known in order to minimize the error.

The Instrumentation Amplifier amplifies (and inverts) the power supply transient at its output. However the amplification factor is limited to 10x due to the limitations mentioned above. A second amplifier is used to increase this range if desired. The input and output of the instrumentation amplifier is plotted in Figure 6. The output from either the instrumentation amplifier or the optional amplifier circuit drives the absolute value circuits. However the original output and it's inverse are needed as inputs to the two absolute value circuits and therefore a Unity Gain Inverter stage is used to invert this output.

The Absolute Value Circuit is shown in the Figure 7. This circuit operates as a full rectifier that produces a unipolar output signal for a given bipolar input signal. Diodes are used as rectifying components connected in the feedback path of an operational amplifier. Signal loss in the diodes due to the high gain of the amplifier is reduced. The input loading problem is addressed by connecting the signal directly to the non-inverting terminal of the op-amp. This circuit is also very sensitive to resistor mismatch, and this causes a gain error where the gain obtained for the positive cycle is different from the gain obtained for the negative cycle. A gain of 1x is achieved in both cycles using the resistor values as shown. By connecting the input to the non-inverting terminals, the output of the circuit becomes a rectified unipolar signal.

This absolute value circuit has a limited high frequency response due to limited slew rate and gain of the opamps and the diode capacitance. The high frequency performance is thus limited by the speed with which an operational amplifier can turn off one rectifying diode and turn on the other. This transition is not instantaneous because the amplifier cannot swing the output voltage instantaneously across the voltage drops of the two diodes.

The rectification of the higher frequency components in the V_{DDT} signals can be improved if two copies of the absolute value circuit are used in parallel, each acting as a half wave rectifier. In this configuration, one copy is used to clip the positive part and one to clip the negative part. The negative supply voltage of the opamps used in these absolute value circuits is reduced so as to eliminate the negative swing in the output voltage. Sufficient bias voltage is still provided at the negative supply to ensure proper operation of the circuit during the positive transitions of the input waveform. The input-output curves for one of the two absolute value circuits is plotted in Figure 8.

A positive DC bias is added to the outputs of the two absolute value circuits. This is required for error control

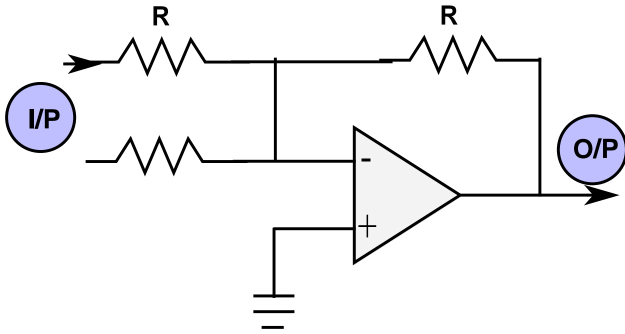


Figure 9. Adder component of the STIC.

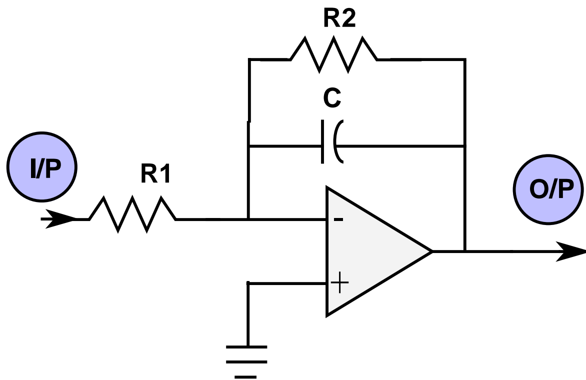


Figure 11. Integrator component of the STIC.

and output stability in the integrator stage of the circuit. The outputs from the two absolute value circuits are passed to the adder circuit that computes the sum of the two signals. The adder circuit is shown in Figure 9. Sample input-output curves are shown for it in Figure 10. The output of the adder circuit is the full unipolar signal which is then passed on to the integrator circuit.

The integration is performed by charging a capacitor connected in the feedback path of an opamp as shown in the integrator circuit in Figure 11. The values of the two resistors and the capacitor are computed depending on the cutoff frequencies desired in this stage. The integrator outputs an analog value (SWA) equal to the area under the difference waveform (SW). The DC bias introduced in the absolute value stage is used to hold the output of the integrator stable. The capacitor used for storing the charge in the integrator starts discharging through the opamp when the input falls to zero. The DC bias on the input signal to the integrator reduces the rate of discharge. Sample input and output simulation results for this circuit are shown in Figure 12.

The cutoff frequencies for the integrator are set according to the frequency range of interest in the V_{DDT} signals. However, the gain of the integrator is frequency dependent

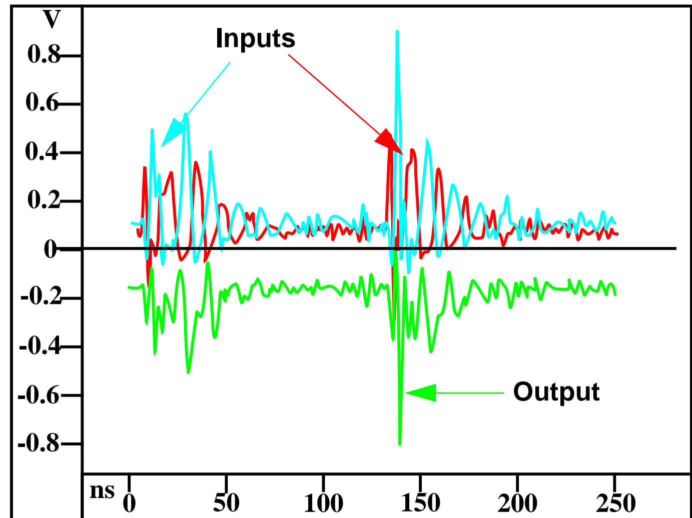


Figure 10. Spice simulation result curves for the adder component.

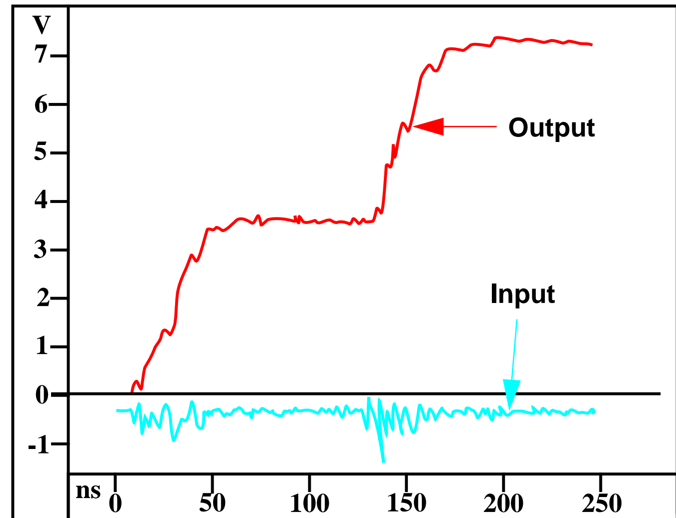


Figure 12. Spice simulation result curves for the integrator component.

and therefore it will generate different values than the DSP technique for the same inputs, as discussed in the next section.

5.0 Experimental Results

Spice simulations are used to test the functionality and the frequency response of the STIC. In these experiments, the inputs to the STIC are a set of V_{DDT} signals generated by a circuit simulated in previous work (see [2] for details). These signals are used because the results of the DSP based analysis are available for comparison. Since the gain of the STIC is frequency dependent, the SWA values generated by the STIC are non-linearly related to those obtained under the DSP technique, so a direct comparison is not possible.

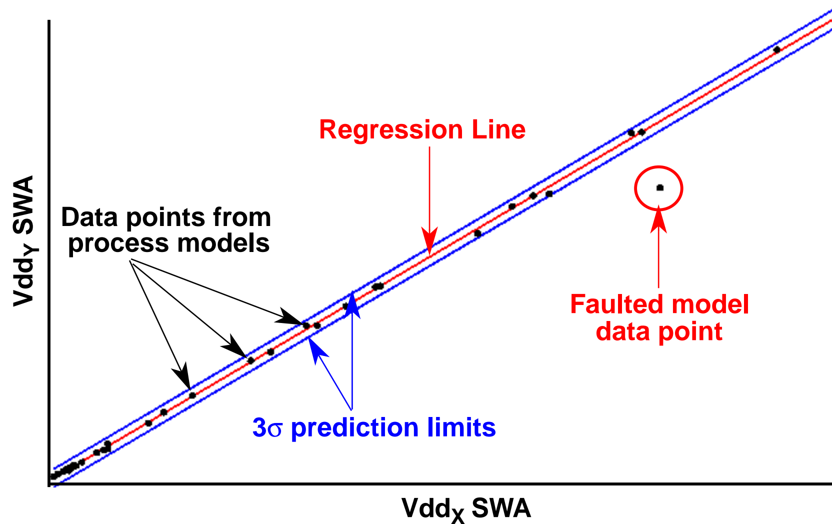


Figure 13. Scatter plot for one pairing of supply pads derived from the STIC output

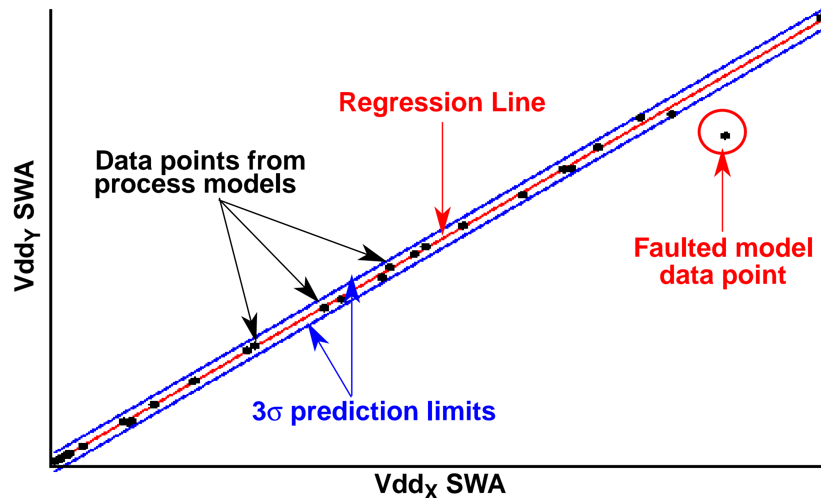


Figure 14. Scatter plot for one pairing of supply pads derived using signal processing technique

However, the regression analysis procedure used in TSA is based on ratios and the absolute magnitudes are only of secondary importance. Therefore, a regression based statistical measure is used to report the accuracy of the STIC in reproducing the output from the DSP technique.

The simulation experiments reported in [2] were conducted on an 8-bit 2's complement multiplier. In these experiments, one reference defect-free circuit model and 40 defect-free process models were designed. In the process models, process variations were modeled through changes in transistor parameters such as Kp, vto etc. and circuit parameters such as poly resistance etc., singly and in combination over the range of +/- 25% the nominal values given in the reference model. In addition one faulted simulation model incorporating a bridging defect was constructed using nominal circuit parameters. A correlation profile (scatter plot, regression line and prediction limits) was derived using the V_{DDT} waveforms from simulations of the 40 defect-free process models for each pairing of power supply pads.

Figure 13 shows the scatter plot derived from the output of the STIC while Figure 14 shows the corresponding scatter plot derived using the DSP technique for one pairing of V_{DD} supply pads, Vdd_x and Vdd_y, under these simulation models. The SWA's computed for Vdd_y from the 41 simulations (40 process, 1 defective) are plotted along the Y axis against those obtained for Vdd_x on the X axis. Since the STIC outputs only one SWA at a time, two STICs are used simultaneously to generate each data point in Figure 13.

In both figures, a regression line ("best-fit line") is drawn through the 40 data points representing the process models. The data points are also delimited by 3σ prediction limits. The data point from the faulted simulation is shown

Supply pad pairing	STIC		DSP		Percentage change in resolution
	Max DF SR	BR SR	Max DF SR	BR SR	
1-2	3.437	31.068	3.359	26.846	113.00%
1-3	3.716	29.561	3.400	24.505	110.30%
1-4	3.654	23.305	3.400	20.266	106.90%
1-5	3.570	25.562	3.337	22.423	106.50%
2-3	3.724	19.270	3.353	21.482	80.75%
3-4	3.862	11.440	3.328	12.423	79.29%
4-5	2.639	21.673	3.750	33.967	90.60%

Table 1: Residual Statistics for a number of supply pad pairings.

below the lower prediction limit in the figures and represents an outlier.

The correlation profiles given by the regression lines and the prediction limits are very similar in the two figures as is the position of the defective data point. However, the relative positions of the data points within the 3σ bands are different. This occurs because the STIC has a non-linear transfer function over a set of frequencies encountered in a V_{DDT} signal and is not able to compute a true integral. Therefore a statistical measure is used instead that is based on residual analysis to compare the correlation profiles generated by the two techniques.

The residual of a given data point is the distance between the data point and the regression line as measured along the Y axis. The residuals of individual data points in the scatter plots are computed and standardized by dividing each residual by the standard deviation of the residuals of defect free data points. The defect free standard deviation is also used to compute standardized residual (SR) for the defective device data point.

Table 1 gives an analysis of the error for several supply pad pairings given by the left most column in the table. For e.g. 1-2 identifies the analysis performed on the residuals for Vdd1 and Vdd2. Columns 2 and 3 give the worst case (Max DF SR) value for the process model SRs and the value computed for the defective model (BR SR).

The difference between the Max DF SR and the BR SR is a measure of the resolution of the test to differentiate between defect-free and defective devices. The ratio of the BR SR and the Max DF SR, expresses the distance of the defective device data point from the regression line in units of the worst case defect free data point. We refer to this ratio as the normalized SR for the defective data point. The fractional change in resolution expressed as a percentage is given by computing the ratio of the normalized SRs for the STIC and the DSP techniques.

The change in the detection resolution of the technique by using the STIC in place of the DSP technique in the worst case is less that 20%. Interestingly in some cases the STIC actually increases the detection resolution.

6.0 Conclusion and future work

A hardware solution is designed to replace the cumbersome laboratory instrumentation and expensive offline processing used to prove the previously published TSA technique.

We have demonstrated the feasibility of the circuit through spice simulations on data collected from simulation experiments. The proposed circuit incorporates 10 opamps and thus may require substantial amount of area when mounted on a probe card. Currently a smaller version of the circuit is being designed. More specifically discrete components are being considered as a means of improving the frequency response of the smaller version. A circuit that includes additional functionality is also under consideration. In this case the dual STIC implementation can be replaced by adding a stage that computes the ratios of the areas directly. In the future, we intend to compare spice results to a hardware implementation of the STIC.

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