Real-Time Hardware Decision Circuit for Transient Signal Analysis

EXTENDED ABSTRACT

Chintan Patel and Jim Plusquellic

Department of CSEE, University of Maryland, Baltimore County

Abstract

Transient Signal Analysis is a parametric device testing method used to detect defects. In this paper we propose a hardware solution as a means of increasing the practicality of TSA in a production environment and to circumvent the time and computational overhead of the existing technique. The proposed circuit monitors transient signals from two power supply pads and computes the area under the waveforms as a test stimulus is applied to the primary inputs. The circuit also computes the ratio of the areas and outputs an analog value. The tester compares this value with a reference value to determine the pass/ fail status of the device. This circuit computes the result in real time and uses the existing capabilities of production testers.

1.0 Introduction

Transient Signal Analysis (TSA) is a parametric approach to testing digital integrated circuits [1][2]. In TSA, defect detection is accomplished by analyzing the transient signals measured at multiple test points of a device. The approach offers two distinct advantages over other logic and parametric testing methods. First, device coupling mechanisms (i.e. power supply) permit the detection of defects at test points that are not directly affected by the defect. Consequently, error observability is greatly enhanced in TSA since they need not be propagated to primary outputs. Second, by cross-correlating the data sampled from multiple test points, false detects caused by mistaking signal variations resulting from process drift as signal variations resulting from defects, are reduced. In fact, all useful parametric test methods must address this problem. The proposed technique works because the effects of process drift tend to be global, changing circuit parameters uniformly across the entire die (or very large portions of it). Hence, the corresponding change in the transient response of the device produces signal variations that are correlated at all test points on the die. In contrast, signal variations caused by a defect tend to be regional with larger amplitudes at test points closer to the defect site. This results in a change in the cross-correlation profile. The RC attenuation effects of the device coupling mechanisms reduce the amplitude of the variation as a function of distance from the defect site.

A significant issue with the TSA technique is the computational complexity of signal collection and post processing. Whole transient waveforms from different test points are collected using sampling and digitizing techniques and analyzed. This technique adds additional time and computer resources to the overhead of conducting the test. In this work, a hardware solution is proposed that is more attractive in the production environment and is compatible with production test equipment.

The proposed circuit measures and computes the areas under the time domain waveform from two test points and outputs an analog value that represents their ratio. The inputs to this circuit are taken directly from the supply pads during wafer probe. The transients, produced as test vectors are delivered to the circuit, are integrated by

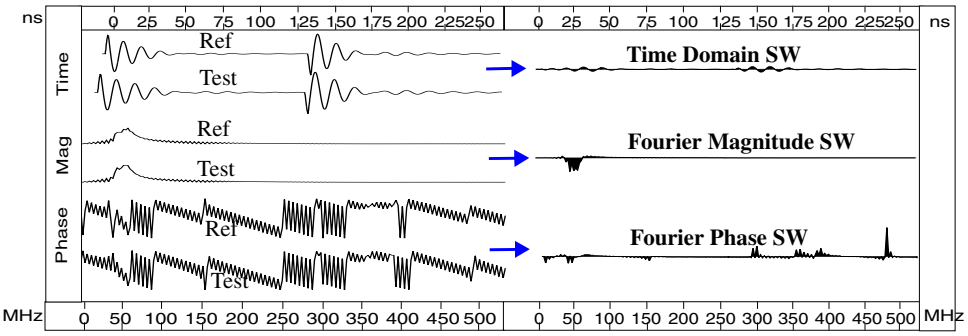

Figure 1. Time a gnature Waveforms.

high frequency operational amplifiers. ' posed circuit is controlled by the tester synchronized with the test patterns it This analog output value is compared w erence value through a tester channel in make the testing decision. The differen values plus or minus a threshold determines the pass/fail status of the device. This circuit replaces high speed digitizing equipment used by the current TSA implementation with real time analog components. The benefits are low cost and reduced response time and complexity of this analysis. We will refer to this circuit as the Area-Ratio Circuit (ARC) in the sections that follow.

The rest of this paper is organized as follows. Section 2.0 outlines some related work. Section 3.0 describes the TSA method. Section 4.0 presents preliminary results. Section 5.0 summarizes our conclusions and areas for future investigation.

2.0 Background

This section will be filled in on the final version of the paper, if accepted. References[3]-[8]

3.0 TSA Method and Model

TSA identifies defective devices by cross-correlating the waveforms measured simultaneously at topologically distinct locations on the device as a test sequence is applied to the primary inputs. The coupling model of digital devices provides the mechanism and the cross-correlation of multiple test point waveforms provides the means by which TSA can distinguish between defect-free and defective devices. The power supply, internodal coupling capacitances, ɔling and substrate coupling create an ork in a digital device which are the ms by which signal variations at a logic . due to the presence of a defect) induce iations at test points on the power supe variations are regional since the RC network attenuates them as a function of distance from the defective node. Therefore, the signals measured at multiple test points can be cross-correlated to detect a defect by analyzing the differences in signal magnitude and phase at the test points. However, signal variations also result from changes in fabrication process parameters, making it difficult to isolate the variations caused by defects. Thus, an important issue is to differentiate between variations due to defects versus those due to process drift. The inability to do so can result in yield loss. In previous work, we determined that signal variations caused by changes in the process tend to be global and measurable in all test point signals [1][2]. More importantly, the signal variations caused by process are proportional across the test points, making it possible to attenuate them using simple signal post-processing techniques. The cross-correlation technique described below is able to calibrate for variations caused by the process and significantly improve the defect sensitivity of the method.

3.1 Signature Waveforms

The present TSA method is based on the analysis of signal differences between a defect-free reference device and a test device. It is assumed that using the raw waveforms measured from the power supply by the ARC will cause a minimal

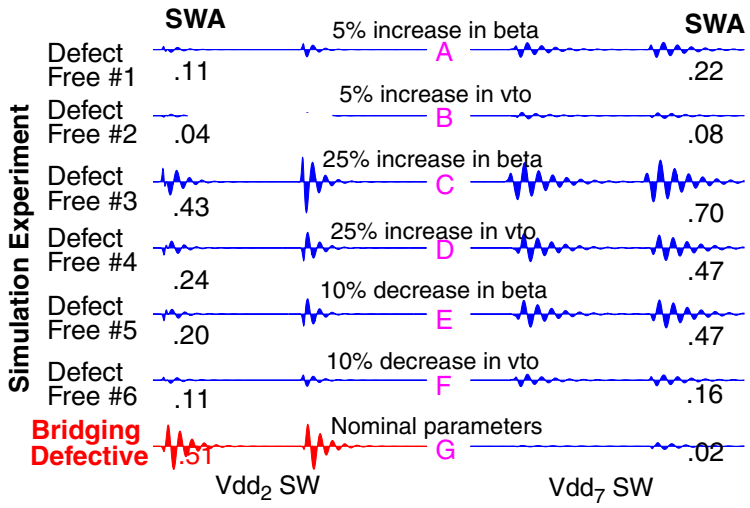

Figure 2. Vdc m 7

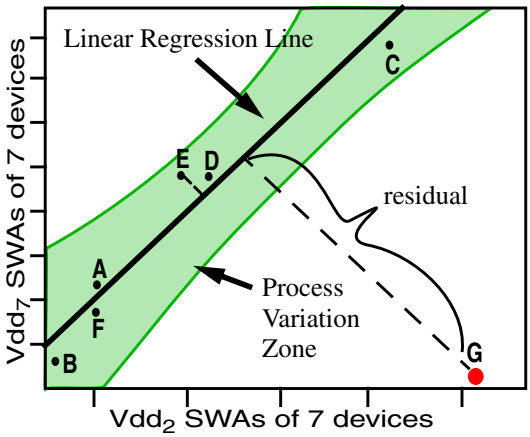

Figure 3. Scatter Plot, Regression Line and Confidence Band using data from Figure 2.

difference in the analysis. Signature Waveforms (SWs) are described here in order to explain pass/fail linear regression analysis in the next section which is the most critical part of the test. However, the raw waveforms measured by the ARC will be substituted in the hardware implementation analysis. SWs are created by subtracting the waveform measured from some test point on the test device from the waveform measured from the same test point location on the reference device. An example is shown in Figure 1. The V_{DD} waveform from the reference (Ref) is shown along the top left plot while the V_{DD} waveform from a test device (Test) is shown below it. Subtracting the test waveform from the reference creates the Time Domain Signature Waveform shown along the top right of Figure 1. The SW is shown shaded to a zero baseline. This area corresponding to the shaded region is used in the statistical analysis to identify defective devices. The area under the curve, computed by evaluating the integral of the waveform using the trapezoidal rule formula over the time interval 0-250ns, is referred to as the Signature Waveform Area (SWA). This area will be instantaneouly computed by ARC.

The effectiveness of the SWAs in capturing the signal variations observable in the SWs is evaluated separately in the time and frequency domain. For the latter case, the raw time domain transient waveforms are used as input to a Discrete Fourier Transform (DFT). The frequency components (both Fourier Magnitude and Fourier Phase) computed by the DFT of the reference and test waveforms are used to create the frequency domain SWs as shown in middle and bottom left of Figure 1.

3.2 Pass/Fail Linear Regression Analysis

Linear regression is used to decide the pass/fail status of a test device. Using a set of SWs from simulations, Figures 2 and 3 illustrate the procedure and the properties exploited in TSA. Figure 2 shows two columns of SWs from two test points (Vdd_2 and Vdd_7). The pairs of SWs in the top 6 rows correspond to different simulation experiments designed to model simple changes in the process. These simulation experiments were performed on different models of the circuit in which exactly one of either beta or vto was varied globally from the nominal value by the amount shown in the figure. The last row shows the SWs from a bridging experiment. The model used in this "faulted" simulation is identical to the model used in the reference except for the presence of the defect. Other than these differences, all other parameters and conditions are identical for these simulations, including the test sequence.

The SW pairs in the first 6 rows are correlated. In other words, the magnitude of the variations in the SWs of one row is proportional to corre-

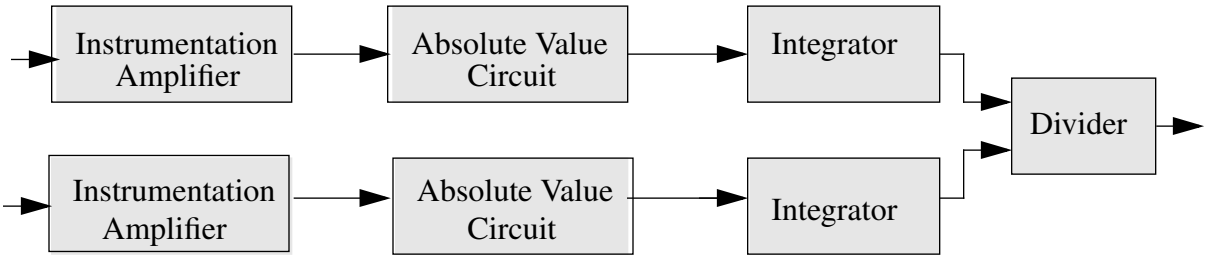

Figure 4. Block Diagram of the Area Ratio Circuit

sponding SWs in other rows. This correlation exists in the raw waveforms as well, and this is the basis for using raw waveforms only in the ARC implementation of TSA. The SWAs shown on the far right and far left in the figure capture this correlation. For example, the SWAs for Vdd_2 and Vdd_7 in Defect-Free simulation experiment #1 are 0.11 and 0.22, respectively. These are proportional to the values 0.04 and 0.08, computed for Vdd_2 and Vdd_7 in Defect-Free simulation experiment #2. The Scatter Plot in Figure 3 plots the SWAs of Vdd_2 (x-axis) against the SWAs of Vdd_7 (y-axis) and illustrates that the SWAs from experiments 1 through 6 track linearly. Thus, a least squares estimate of a linear regression line (best fit line) shown in the figure tracks process variation in data points A through F. The shaded region around the regression line is called the Process Variation Zone and is delimited by a 99.9% (3σ) confidence band. The Process Variation Zone is wider than the data points it encloses and accounts for small non-linearity, measurement noise and intra-device process variations. The Process Variation Zone defines the pass/fail threshold of the ratio computed by the ARC.

In contrast, the SWs labeled G shown along the bottom of Figure 2 are not proportional to the SWs in the other rows. In this case, the defect has produced regional variation in the SW of Vdd_2 due to its proximity to this supply rail. A much smaller amount of variation occurs in Vdd_7 due to the attenuation effect of the RC network. The lack of correlation in this pairing is illustrated by the outlier data point G in Figure 3. From the plot, it is clear that the behavior of this device is not characteristic to the norm defined by the regression bounds of the Defect-Free simulation experiments.

Based on this example, the pass/fail criterion under each test sequence is straightforward. Across all pairings of test points, if a test device generates a ratio that falls outside of the Process Variation Zone for any pairing, the test device is defective. A defective device is expected to produce at least one data point with ratio greater than the threshold. This is the expected result since the variation generated by the defect is regional. In other words, some ratios from defective devices may fall in the passing range. Therefore, in the worst case, it may be necessary to analyze all pairing of test points in order to determine if the test device passes under the test sequence.

This procedure has been demonstrated in previous works [1] [2]. The main deficiency is the hardware requirements for signal collection and post processing. A more attractive solution to its implementation is through the use of a dedicated analog circuit capable of performing the equivalent function that can be easily interfaced with existing tester technology. The next section presents one such solution.

4.0 Experiment Method

4.1 Overview of the Area ratio circuit (ARC)

The block diagram of the area ratio circuit is shown in figure 4.The two inputs to the circuit are signals measured from two wire bonded pads that connect to the core logic power supply rails. The transients generated as a test sequence is applied to the primary inputs are DC biased at 5V. The

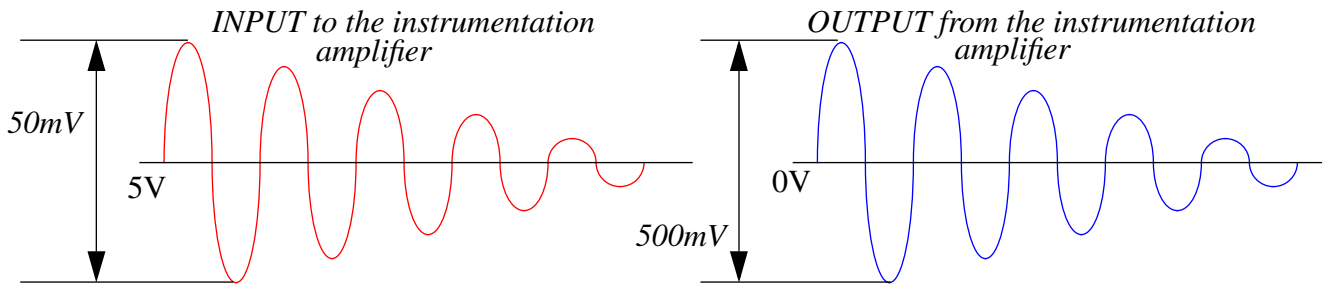

Figure 5. Ideal Input Output curves for the instrumentation amplifier stage of ARC.

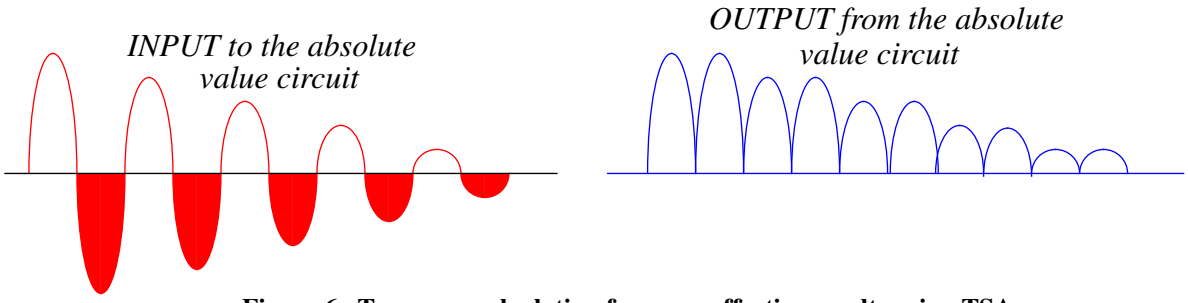

Figure 6. True area calculation for more effective results using TSA.

first stage of the ARC (instrumentation amplifier) removes this bias and amplifies the transient signals. This is necessary because the range of variations in the transient signals is small. In previous experiments, we found these values vary over +/- 50mV. Increasing this range to +/- 500mV permits a more robust implementation of the components in later stages. This transformation step is illustrated in Figure 5. The ideal output from the instrumentation amplifier is shown on the right.

TSA is most effective if the area used in the analysis is the sum of the areas under the positive portion of the transient waveform plus the absolute value of the area under the negative portion. The absolute value component in the second stage of the ARC (Figure 4) is responsible for converting the transient to a unipolar form. This circuit receives a bipolar signal and generates a unipolar signal as shown in Figure 6. With proper biasing, this component can provide equal gain to both the negative and the positive cylces.

The rectified unipolar signal is now passed to the integrator stage of the ARC in order to compute the total area. Figure 7 shows the ideal transformation step of this component.

The outputs of the two integrators are fed to the divider circuit of the ARC to obtain the ratio of the areas under the two time domain transient signals. This value is output to a tester channel for comparison to a reference. The tester incorporates a tolerance between the measured and reference value as determined by a set of defect- free devices and determines the pass fail status of the test as described previously in section 3.2.

With this overview, several key issues need to be addressed. As indicated previously, the transient signal varies over a relatively small range (50 to 100 millivolts) and this signal is riding on a DC voltage of 5V. The circuit must effectively remove this DC bias while minimizing the degradation in the actual transient signal. Of equal importance is the frequency response of this circuit- its amplifiers, the absolute value circuit and the integrator. These components need to operate over the transient frequency range of interest, which is expected to reach 1GHz. Therefore, the design and analysis of these components are treated differently than the divider circuit which is constructed to operate at the test pattern deliv-

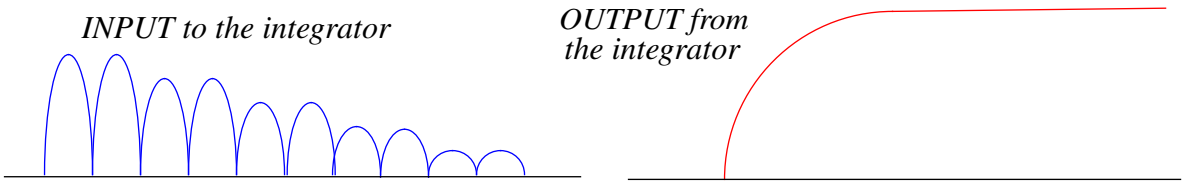

Figure 7. Ideal Input Output curves for the integrator component of ARC.

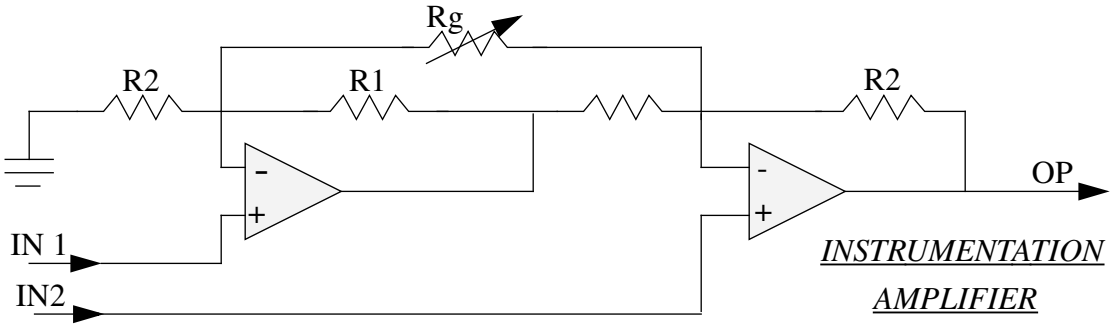

Figure 8. Ideal Input Output curves of the integrator stage of the ARC.

ery rate. For example, the integrator time period must be designed to retain 95% of its initial value over the time period ending with the introduction of the next test pattern. This is necessary because the next stage of the ARC, the divider circuit, operates at lower frequencies and needs this time to complete its computation.

4.2 Details of the ARC

ARC uses opamps as its basic building blocks. The first stage of the ARC removes the 5V DC bias using the configuration shown in Figure 8.

This circuit is a differential amplifier with a biasing configuration to allow effective amplification of signals up to 100mV. The first operational amplifier in the circuit acts as an non-inverting amplifier for the input IN1. The output of this op-amp is fed to the next opamp which acts as an inverting amplifier. The second input IN2 to the circuit is a fixed DC voltage of 5V. The variable resistor Rg is the gain control resistance of the circuit. To ensure linearity, the total gain is set around 10x.

The voltage transfer relationship is given by the following formula

$$\frac{E_0}{E_I} = -\left(1 + \frac{R_2}{R_1} + 2\frac{R_2}{R_G}\right)$$

where E_0 = Output Voltage OP
E_I = (IN 1 - IN2)

In this circuit, the common mode rejection error of the two amplifiers tend to cancel but the other errors like offset bias voltage and error due to input bias current are additive. Therefore, special care is taken when biasing this circuit in order to effectively compensate for these inherent limitations of the opamp. Also, any resistor mismatch causes a non-zero common-mode gain that equals the fractional mismatch.

The instrumentation amplifier amplifies (and inverts) the power supply transient at its output. However the amplification factor is limited to 10x which increases the range to +/- 500mV. A second (inverting) amplifier is used to increase this range to +/- 1V. This voltage range allows more efficient operation of the following absolute value stage of the ARC. However, direct connection of the instrumentation amplifier to the inverting

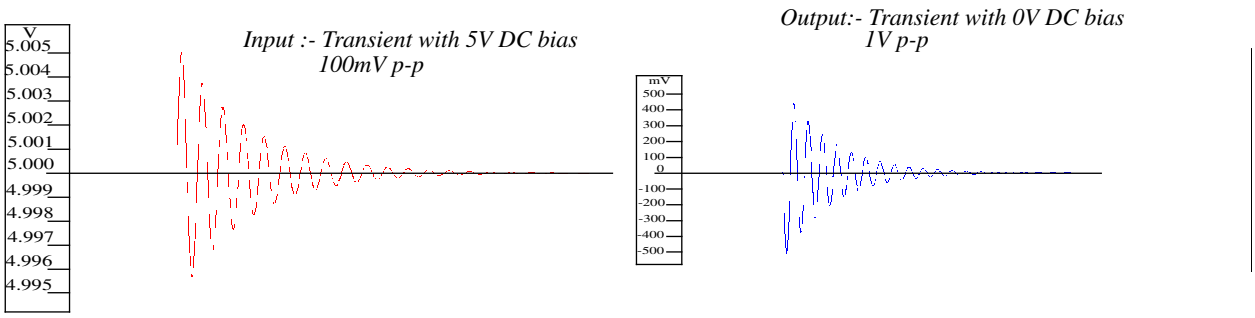

Figure 9. Instrumentation Amplifier component of the ARC

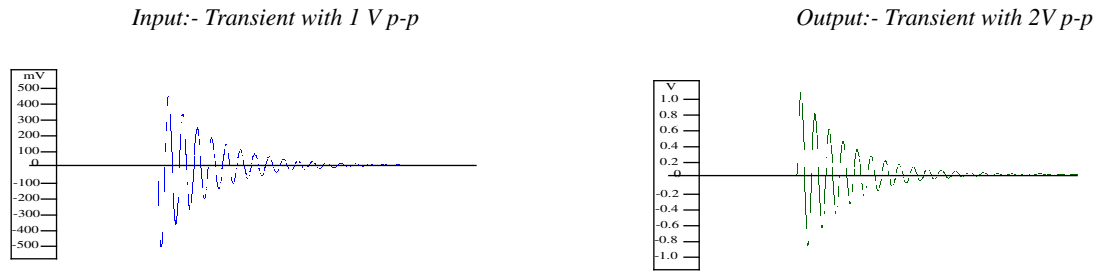

Figure 10. Spice Simulation Results for the instrumentation Amplifier

amplifier will adversely load the instrumentation amplifier. In this case the output of the instrumentation amplifier will see the low input resistance of the gain control resistor of the inverting amplifier as the input resistance of the inverting amplifier. Instead a voltage follower stage is connected in between the instrumentation amplifier and the inverting amplifier in order to increase the load resistance seen by the instrumentation amplifier to a value larger than 1MΩ.

Spice simulations were run on each of the components of the ARC. These simulations were run to verify the feasibility of various components of the ARC. Optimizations will be made in the final version of this circuit. The simulations were run using generic bipolar transistor spice models. Due to the lack of adequate spice models the simulations were run at 10KHz. Future work will include BJT models for 0.5µ or any other current technologies as well as running the simulations again in the MHz range. The aim is to make the circuit viable for testing chips running at 500MHz. The input and output of the instrumentation amplifier is plotted in the Figure 9. The plot show that the input is a 100mV peak-to-peak signal riding on a DC bias of 5V. The instrumentation amplifier is biased to give a gain of 10x to the input. The output from the circuit is a transient having 1V p-p and a DC bias of 0V. This signal is fed, through the voltage follower stage, to the inverting amplifier. The input and output from this stage of the ARC is plotted in the Figure 10. The gain of this stage of the ARC is set at 2x. The output is a transient signal with 2V p-p value which is the required voltage level for the proper operation of the preceding stages of the ARC.

The inverting amplifier drives the absolute value circuit that rectifies the negative portions of the transients. The absolute value circuit is shown in the Figure 11.

Diodes are used as rectifying components connected in the feedback path of an operational amplifier. Signal loss in the diodes due to the high gain of the amplifier is reduced. The loading problem is addressed by connecting the signal directly to the non-inverting terminal of the op-amp. This circuit is also very sensitive to

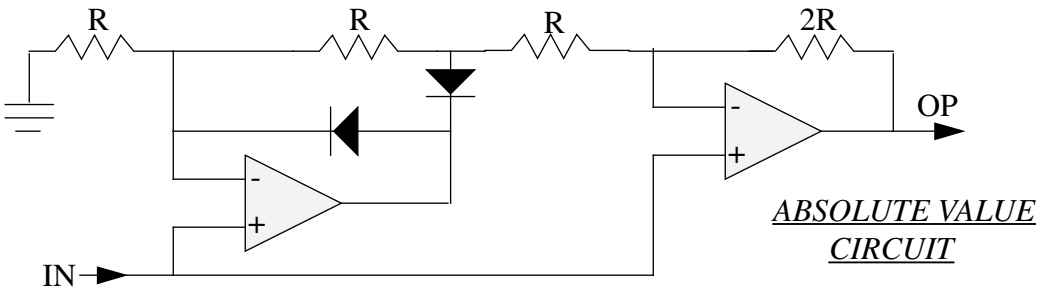

Figure 11. Spice simulation results for inverting amplifier

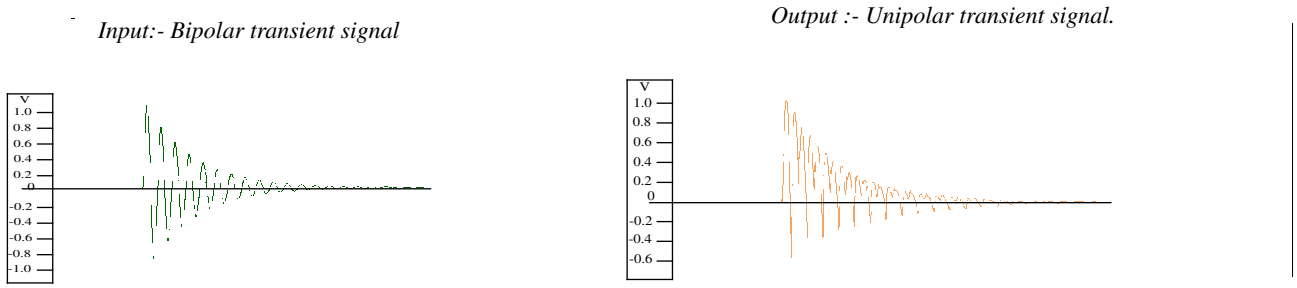

Figure 12. Absolute Value Component of the ARC

resistor mismatch, and this causes a gain error where the gain obtained for the positive cycle is different from the one obtained for the negative cycle. A gain of 1x is achieved in both cycles using the resistor values as shown. By connecting the input to the non-inverting terminals the output of the circuit becomes a rectified unipolar signal.

The spice simulation results for the absolute value component of the ARC are plotted in the Figure 12. The input to this circuit comes from the output of the inverting amplifier stage of the ARC. The output plot shows that the bipolar input signal is converted into a unipolar signal. By matching the resistors exactly as shown in Figure 11 a gain of 1x is obtained for both the negative and positive cycles of the input waveform. The overshoots into the negative voltage range is the error of this circuit, and these need to be eliminated in the final implementation.

The output of the absolute value circuit is fed to a voltage follower, which in turn drives the simple integrator circuit. The configuration of the integrator circuit allows the output to remain at 95% of its initial value in order to give the divider circuit time to perform its operation. The spice simulation results for the integrator are plotted in Figure 13. The input to the integrator is the output signal from the absolute value circuit. The output of the integrator is held at nearly 95% of its initial value over a considerable period of time even after the transient signal input dies out. This ensures the proper operation of the divider stage of the ARC which is designed to operate at a low rate equal to that of the test pattern application.

The divider circuit computes the ratio of two voltages. The divider circuit is shown in the Figure 14. The divider circuit uses FETs that are driven by the feedback amplifier. Below pinchoff the FETs behave as voltage controlled resistors which are controlled by their gate voltage. This property of the FETs is used to compute the ratio. Also, the resistances of the FETs are sensitive to their drain-source signal voltage. Therefore if the input signals X and Z are too far apart a mismatch in FET resistances will occur and a corresponding divider linearity error of several percent will

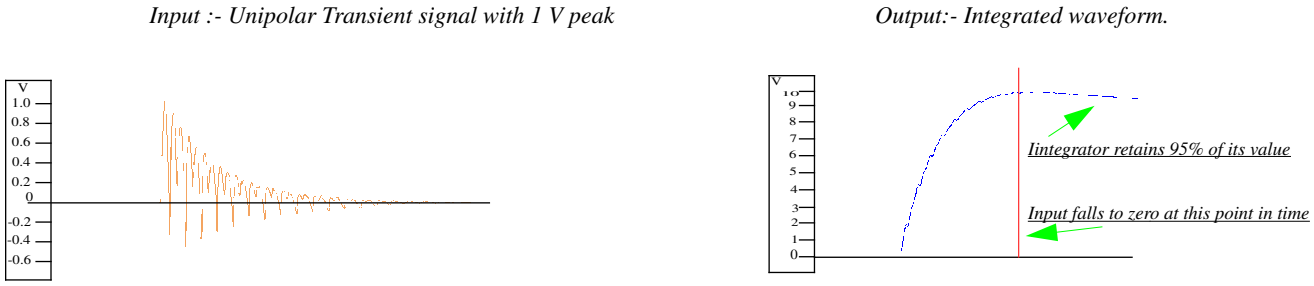

Figure 13. Spice simulation results for absolute value component of ARC.

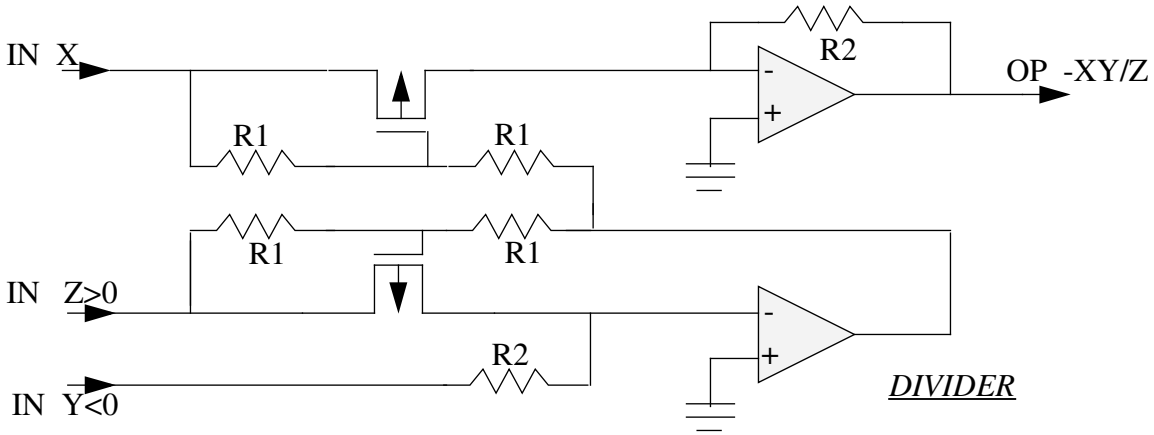

Figure 14. Divider Component of the ARC.

result. The areas under the transient waveforms are likely to be similar because of the low resistance of the interconnect between the supply pins, and the source of error is expected to be small. As an additional countermeasure a feedback path through resistor R1 in the Figure 14 is used to reduce the signal voltages on the FET sources, thereby reducing the error. This circuit is very sensitive to the input errors of the op-amps such as input offset voltage and input bias voltage. Therefore, special care is taken when biasing this circuit to eliminate this error. In the final version of the paper, the errors of the ARC will be computed with a maximum target set at about 5%

5.0 Conclusion and areas of future investigation

In this paper, we proposed a hardware solution that addresses the practicality of implementing a parametric device testing method called Transient Signal Analysis. The hardware solution is designed to replace the digitizer and sampling requirements, thereby reducing the time and computer resources of the current TSA method. The proposed circuit is designed to allow much higher tester pattern delivery rates than currently possible as well as interface effectively with existing tester technology.

We have demonstrated the feasibility of the circuit ar low frequencies (10KHz) through spice simulations. We are exploring the possibility of adapting the circuit for higher frequency operations. We will present extensive simulation results in the final version of this paper that investigates the frequency response and accuracy of design using transistor models from more advanced technologies. We are looking at several implementations of operational amplifiers which

are the basic building blocks of all the components of the ARC and are experimenting with both BJT and MOS transistor based operational amplifiers. Simulations so far have been carried out using very generic BJT transistor models. We are awaiting BJT transistor models from current technologies to simulate the ARC. The final paper shall present the actual hardware implementation of the circuit either using discrete components or as an on chip circuit. The frequency response available from each of this techniques will be the final criteria for selection of the proper implementation of this circuit. Also we are reviewing literature listed in the reference and hope to extract circuit optimizations that have been proven reliable.

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