

Custom Hardware Circuit for Power Supply Transient Signal Analysis

Chintan Patel, Jim Plusquellic and Fidel Muradali

In this paper, we propose a circuit that computes the area under a difference waveform and produces its analog value as output. The transient waveforms pair from which the difference is computed is given as input to the circuit. The circuit is proposed as a hardware solution for a device testing technique called Transient Signal Analysis.

Introduction: Defect detection in Transient Signal Analysis (TSA) is accomplished by analyzing the transient signals measured at multiple test points of a device. A simple correlation procedure is used as a means of making the technique tolerant to normal variations in fab process parameters. The correlation technique applies signal processing algorithms to a digitized representation of the waveforms. Although the computational complexity of the routines is small, equipment capable of digitizing transient waveforms does not fit well into the traditional model of a production test environment. The proposed hardware circuit is designed to replace the digitizing equipment and perform the signal processing using analog circuit design elements. The circuit is designed to compute a time domain difference waveform from a pair of transient input waveforms measured from the supply pads of two devices during wafer probe. The area under this difference waveform is output as an analog value to the tester. The circuit is controlled by

the tester and is thus synchronized with the delivery of the test patterns. This enables the tester to determine the pass/fail status of the device by simply comparing this value to a predetermined threshold as specified by the TSA method. The circuit uses high frequency operational amplifiers to perform the integration thus circumventing the need for high speed digitizing equipment and thereby reducing cost, time and complexity of the test. The circuit is referred as a Supply Transient Integration Circuit (STIC) in the sections that follow.

TSA Method: TSA identifies defective devices by cross-correlating the waveforms measured simultaneously at topologically distinct locations on the device [1][2]. Signal variations caused by changes in the process tend to be global and measurable at all test points whereas those due to a defect are regional and measurable only at a subset of the test points [1][2]. Therefore, the signals measured at multiple test points can be cross-correlated to detect a defect by observing an anomaly in the correlation profile of the test device. The correlation profile is obtained from a set of defect-free devices. First the areas under the difference waveforms (Signature Waveforms) are computed by subtracting the transient waveforms at a given supply pad on the defect-free test device from the corresponding waveform on a defect-free reference device [1][2]. The correlation profile is derived using linear regression analysis of scatter plots which plot these areas pairwise from two supply pads. A least squares estimate of the linear regression line is derived through the data points and a Process Variation Zone around the regression line is derived to account for process variations effects. The procedure then determines the pass/fail status in production test of untested devices by evaluating the position of the test device data

points in the correlation profile given by the scatterplot. This procedure has been demonstrated in previous works [1][2].

Supply Transient Integration Circuit (STIC): The block diagram of the STIC is shown in Figure 1 along with the input and output waveforms for each component of the circuit.

The two inputs to the circuit are signals measured from a supply pad that connects to the core logic power supply rail for a test device and a reference device. The transients generated as a test sequence is applied to the primary inputs are DC biased at the supply voltage. The first stage of the STIC (instrumentation amplifier) removes this bias by computing the difference between the test and reference transient waveforms. This circuit is a differential amplifier with a biasing configuration to allow effective amplification of signals up to 100mV. The instrumentation amplifier amplifies (and inverts) the power supply transient at its output with an amplification factor that is limited to 10x. A second inverting amplifier may be used to increase this range if desired as shown in Figure 1.

TSA is most effective if the area used in the analysis is the sum of the areas under the positive portion of the transient waveform and the absolute value of the area under the negative portion. Two absolute value circuits are used for this purpose, one driven by the amplified output of the instrumentation amplifier (point 1 in Figure 1) and the other by its inverse (point 2 in Figure 1). Diodes are used as rectifying components connected in the feedback path of an operational amplifier. A single absolute value circuit can be used to convert the bipolar signal into a unipolar signal. However this is not possible for the higher frequencies encountered in the transient signals. Therefore two stages of this circuit are used, one to clip the positive part and one to clip the negative part. The outputs

from the two absolute value circuits are passed to the adder circuit that computes the sum of the two signals as shown at point 3 in Figure 1. The output of the adder circuit is the full unipolar signal which is then passed on to the integrator circuit to compute the total area under the curve. The integration is performed by charging a capacitor connected in the feedback path of an opamp. The integrator outputs an analog value equal to the area under the signature waveform as shown at point 4 in Figure 1. This value is then fed to a tester channel for comparison to a threshold, as discussed previously.

Results: Spice simulations were run to test the functionality and the frequency response of the circuit. The transients used as input were collected from simulations on an 8-bit 2's complement multiplier circuit. The device has 10 power supply pads from which the transients are collected. One reference defect-free simulation and 40 defect-free simulations with process variations were run and the transients collected were given as input to the circuit. Process variations were modeled through changes in transistor parameters such as beta, v_{to} etc. and circuit parameters such as poly resistance etc. singly and in combination over the range of $\pm 25\%$ the nominal values. One bridging experiment simulation was run using the nominal circuit parameters. A correlation profile was derived using the data points from the 40 defect-free simulations for each pairing of power supply pads. Figure 2 shows one such scatter plot obtained for two supply pads Vdd1 and Vdd2. The regression line (marked as 1 in Figure 2) is derived through the 40 defect free data points. The Process Variation Zone (PVZ) is delimited using 3σ prediction bands labeled as 2 and 3 in the figure. Marker 4 shows the position of an outlier, the defective device data point. Since the data points falls outside the PVZ, it can be used to identify the test device

as defective. The error was less than 10% when compared to the technique which uses the signal processing technique originally defined for TSA. In this analysis, the error is computed as the relative positional differences in the data points from the respective regression lines. Further verification of the STIC was performed using the data from other simulations and is not reported here due to space limitations. Reference [1] and [2] describe these simulation experiments.

Conclusions: In this paper, we proposed a hardware solution that addresses the practical aspects of implementing a parametric device testing method called Transient Signal Analysis. A hardware circuit is proposed that is capable of performing the data collection and signal processing operations for TSA with less than 10% error. The proposed circuit is designed to allow much higher tester pattern delivery rates than is currently possible and interfaces well with existing tester technology. We verified functionality and accuracy of the circuit through spice simulations. The circuit proposed is built from discrete components. Current work is focussed on developing the integrated version that can be easily interfaced with existing probe card technologies.

References

- [1] James F. Plusquellic, Donald M. Chiarulli, and Steven P. Levitan. "Characterization of CMOS Defects using Transient Signal Analysis," *DFT*, pp. 93-101, November, 1998.
- [2] Amy Germida, Zheng Yan, J. F. Plusquellic and Fidel Muradali. "Defect Detection using Power Supply Transient Signal Analysis," In proceedings *International Test Conference*, 1999, pp. 67-76.

[3] Stopjakova, V; Manhaeve, H; Sidiropulos, M. "On-chip transient current monitor for testing of low-voltage CMOS IC," Design, Automation and Test in Europe Conference and Exhibition, 1999. Cat. No. PR00078 p.xxx+798,538-42.

[4] Sidiropulos, M; Stopjakova, V.; Manhaeve, H. "Implementation of BIC monitor in balanced analogue self-test" Electronics Letters, vol.32, no.20 p. 1841-2, Sept. 1996.

[5] Stopjakova, V; Butas, J.; Durackova, D. "An on chip supply current sensor for dynamic testing of CMOS ICs," Journal of Electrical Engineering, vol.49, no.3-4 p.91-6, 1998.

Authors' affiliations:

Chintan Patel (cpatel2@cs.umbc.edu) and James Plusquellic (plusquel@cs.umbc.edu)
(Computer Science and Electrical Engineering Department, University of Maryland Baltimore County, 1000 Hilltop Circle, ECS Building, Baltimore, Maryland 21250, USA).

Fidel Muradali (fidel_muradali@agilent.com)

(Agilent Technologies Inc., Santa Clara, California, USA)

Figure captions:

Figure 1: Block Diagram of the Supply Transient Integration Circuit (STIC).

I: Inputs to the circuit. Upper waveform is the reference device transient and lower the test device.

1: Input to 1st absolute value circuit. **2:** Input to 2nd absolute value circuit.

3: Unipolar output of the adder circuit. **4:** Analog integrated value as final output.

Figure 2: Scatter plot for one pairing of supply pads (Vdd1 and Vdd2 in this case).

1: Regression Line computed using 40 data points. **2:** Upper prediction band.

3: Lower prediction band. **4:** 1 defective device data point.

Figure 1

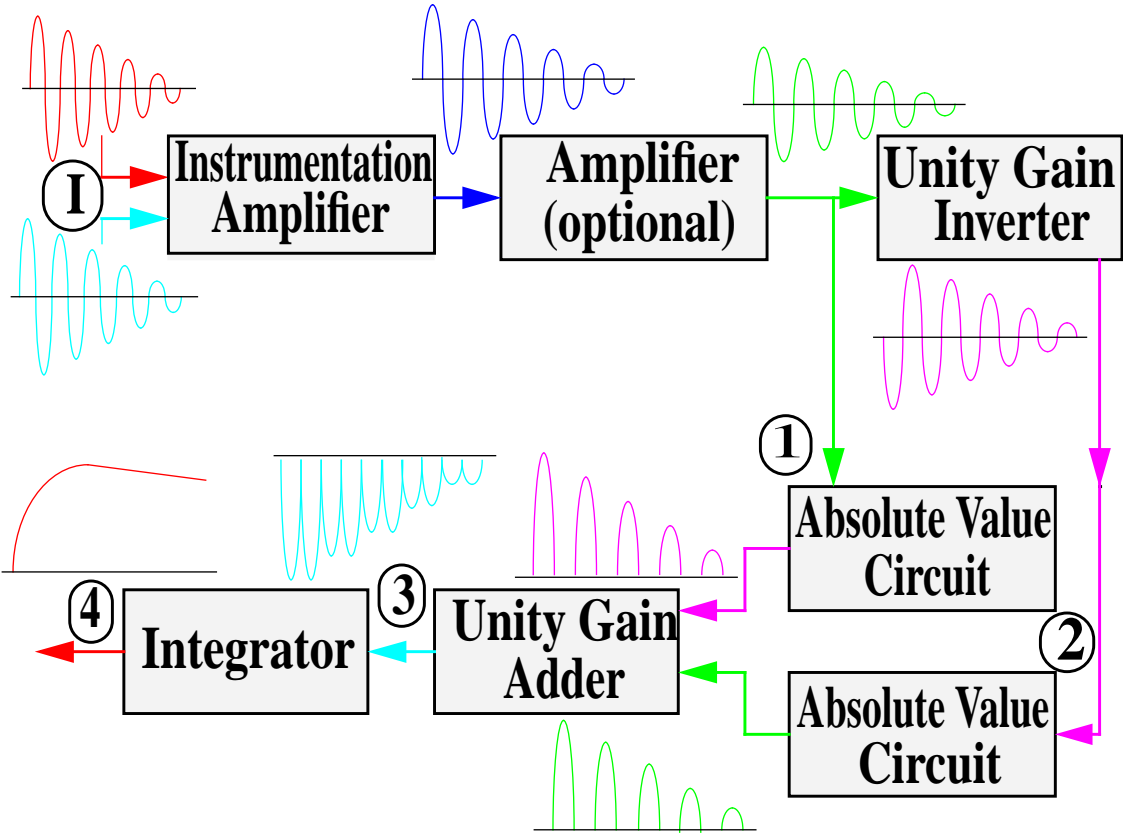


Figure 2

