8-bit Multiplier Simulation Experiments Investigating the Use of Power Supply Transient Signals for the Detection of CMOS Defects

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Abstract

Transient Signal Analysis is a digital device testing method that is based on the analysis of voltage transients at multiple test points. In this paper, the power supply transient signals from simulation experiments on an 8-bit multiplier are analyzed at multiple test points in both the time and frequency domain. Linear regression analysis is used to separate and identify the signal variations introduced by defects and the variations caused by changes in fabrication process parameters. Defects were introduced into the simulation model by adding material (shorts) or removing material (opens) from the layout. Process parameter fluctuations were modeled by randomly varying transistor and circuit parameters individually and in groups over the range of +/- 25% of the nominal parameters. The results of the analysis show that it is possible to distinguish between defect-free devices with injected process variation and defective devices.

1.0 Introduction

Transient Signal Analysis (TSA) is a parametric approach to testing digital integrated circuits [1][2]. In TSA, defect detection is accomplished by analyzing the transient signals measured at multiple test points of a device. The approach offers two distinct advantages over other logic and parametric testing methods. First, device coupling mechanisms (i.e. power supply) permit the detection of defects at test points that are not directly affected by the defect. Consequently, error observability is greatly enhanced in TSA since they need not be propagated to primary outputs. Second, by cross-correlating the data sampled from multiple test points, false detects caused by mistaking signal variations resulting from process drift as signal variations resulting from defects, are reduced. In fact, all useful parametric test methods must address this problem. The proposed technique works because the effects of process drift tend to be global, changing circuit parameters uniformly across the entire die. Hence, the corresponding change in the transient response of the device produces signal variations that are correlated at all test points on the die. In contrast, signal variations caused by a defect tend to be regional with larger amplitudes at test points closer to the defect site. The RC attenuation effects of the device coupling mechanisms reduce the amplitude of the variation as a function of distance from the defect site. This results in a reduction in the cross-correlation profile of the device. A simple statistical method is presented that detects the absence of correlation in one or more test point signals of defective devices while attenuating the signal variations that are correlated or caused by changes in the process.

In previous work, the analysis was carried out using the transient signals measured on core logic test pads on the outputs of logic nodes [3]. Core logic test pads are contact opens in the passivation layer to metal below. Although this strategy is sensitive to both logic faults and parametric defects that cause changes in propagation delay, the additional capacitive load introduced by the core logic test pads degrades circuit performance. In this work, the device transient signals are measured at test points on the supply rails instead. Power supply test points are attractive for several reasons. Assuming that the supply rails are the primary coupling mechanism [4], they are more sensitive to signal variations introduced by defects and less intrusive than points in the core logic. Also, due to the ubiquity of the supply rail interconnect, there is a high degree of capacitive coupling between the supply rails and local interconnect, which increases the sensitivity of the test. Lastly, the grid-like regularity of the supply rail interconnect and the distribution of multiple supply pins around the periphery of the device provides regional observability in

existing designs.

In this paper, experiments are designed to determine the effectiveness of analyzing power supply transient signals as a means of identifying defective devices. Multiple versions of an 8-bit multiplier were simulated with bridging and open defects. The results show that it is possible to detect these defects while compensating for injected process variation.

The rest of this paper is organized as follows. Section 2.0 outlines some related work. Section 3.0 describes the TSA method. Section 4.0 presents the experimental setup. Section 5.0 presents experimental results and, finally, Section 6.0 summarizes our conclusions and areas for future investigation.

2.0 Background

Parametric device testing strategies are based on the analysis of a circuit's parametric properties, for example, propagation delay, magnitude of quiescent supply current or transient response [5]. Many types of parametric tests have been proposed [6] but recent research interest has focused on two types I_{DDQ} [7] and I_{DD} [8].

I_{DDQ} is based on the measurement of an IC's supply current when all nodes have stabilized to a quiescent value. I_{DDQ} has been shown to be an effective detection technique for CMOS bridging defects, but is not applicable to all types of CMOS defects [9]. Furthermore, the near-future effectiveness of IDDQ as a defect screen has been questioned because defect currents may be difficult to resolve within the high background leakage of large deep submicron devices (<0.15microns) [10].

Several dynamic supply current I_{DD}-based approaches have since been proposed to overcome the limitations caused by the static nature of the I_{DDQ} test [11][12][13][14][15]. In general, these I_{DD}-based methods are not hampered by the slow test application rates and are not as sensitive to design styles as I_{DDQ}, however they do not provide a means of accounting for process tolerances and are therefore subject to yield loss.

Recent related works show promising results and are based in principle on the process calibration technique that we have proposed [16] and [17]. However, calibration is performed in these techniques across test sequences rather than within a single test sequence. Although these methods are simpler to implement since only one waveform is analyzed per test sequence, it has yet to be determined which of these methods can be adapted to provide adequate defect sensitivities for large deep submicron devices. The multiple test point measurements taken in TSA enhances defect sensitivity at the expense of increased measurement and computational complexity.

3.0 TSA Method and Model

TSA identifies defective devices by cross-correlating the waveforms measured simultaneously at topologically distinct locations on the device as a test sequence is applied to the primary inputs. The coupling model of digital devices provides the mechanism and the cross-correlation of multiple test point waveforms provides the means by which TSA can distinguish between defect-free and defective devices. The power supply, internodal coupling capacitances, well coupling and substrate coupling create an RC network in a digital device which are the mechanisms by which signal variations at a logic node (e.g. due to the presence of a defect) induce signal variations at test points on the power supply. These variations are regional since the RC network attenuates them as a function of distance from the defective node. Therefore, the signals measured at multiple test points can be cross-correlated to detect a defect by analyzing the differences in signal magnitude and phase at the test points. However, signal variations also result from changes in fabrication process parameters, making it difficult to isolate the variations caused by defects. Thus, an important issue is to differentiate between variations due to defects versus those due to process drift. The inability to do so can result in yield loss. In previous work, we determined that

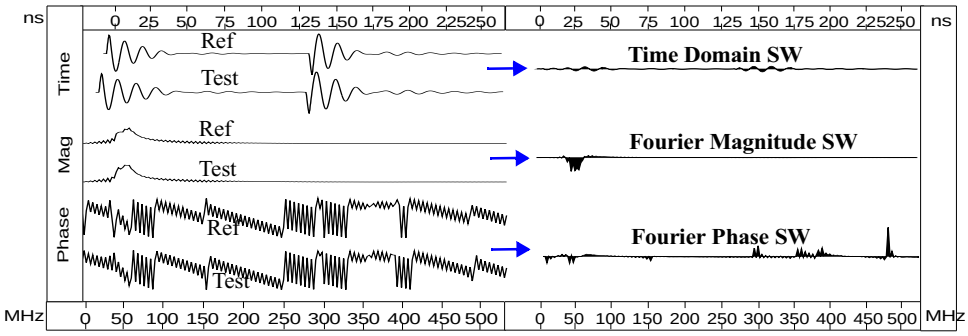

Figure 1. Time and Frequency Domain Signature Waveforms.

signal variations caused by changes in the process tend to be global and measurable in all test point signals [1]. More importantly, the signal variations caused by process are proportional across the test points, making it possible to attenuate them using simple signal post-processing techniques. The cross-correlation technique described below is able to calibrate for variations caused by the process and significantly improve the defect sensitivity of the method.

3.1 Signature Waveforms

TSA is based on the analysis of signal differences between a defect-free reference device and a test device. Signature Waveforms (SWs) capture these differences. SWs are created by subtracting the waveform measured from some test point on the test device from the waveform measured from the same test point location on the reference device. An example is shown in Figure 1. The V_{DD} waveform from the reference (Ref) is shown along the top left plot while the V_{DD} waveform from a test device (Test) is shown below it. Subtracting the test waveform from the reference creates the Time Domain Signature Waveform shown along the top right of Figure 1. The SW is shown shaded to a zero baseline. The area under the curve, computed by evaluating the integral of the waveform using the trapezoidal rule formula over the time interval 0-250ns, is referred to as the Signature Waveform Area (SWA). A similar process is performed in the frequency domain as shown in middle and bottom left of Figure 1. The areas of the shaded portion of the Fourier Magnitude SW and Fourier Phase SW are computed over the range of 0-200 MHz.

3.2 Pass/Fail Linear Regression Analysis

Linear regression is used to decide the pass/fail status of a test device. Using a set of SWs from simulations, Figures 2 and 3 illustrate the procedure and the properties exploited in TSA. Figure 2 shows two columns of SWs from two test points (Vdd_2 and Vdd_7). The pairs of SWs in the top 6 rows correspond to different simulation experiments designed to model simple changes in the process. These simulation experiments were performed on different models of the circuit in which exactly one of either beta or vto was varied globally from the nominal value by the amount shown in the figure. The last row shows the SWs from a bridging experiment. The model used in this "faulted" simulation is identical to the model used in the reference except for the presence of the defect. Other than these differences, all other parameters and conditions are identical for these simulations, including the test sequence.

The SW pairs in the first 6 rows are correlated. In other words, the magnitude of the variations in the SWs of one row is proportional to corresponding SWs in other rows. The SWAs shown on the far right and far left in the figure capture this correlation. For example, the SWAs for Vdd_2 and Vdd_7 in Defect-Free simulation experiment #1 are 0.11 and 0.22, respectively. These are proportional to the values 0.04 and 0.08, computed for Vdd_2 and Vdd_7 in Defect-Free simulation experiment #2. The Scatter Plot in Figure 3 plots the SWAs of Vdd_2 (x-axis) against the SWAs of Vdd_7 (y-axis) and illustrates that the SWAs from experiments 1 through 6 track linearly. Thus, a least

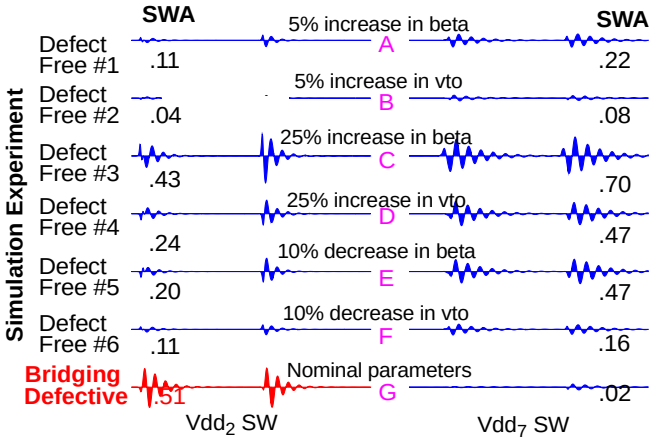

Figure 2. Vdd_2 and Vdd_7 Signature Waveforms from 7 simulation runs.

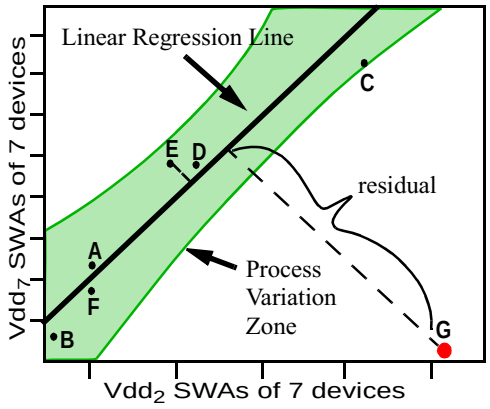

Figure 3. Scatter plot, regression line and prediction limits using data from Figure 2.

squares estimate of a linear regression line (best fit line) shown in the figure tracks process variation in data points A through F. The shaded region around the regression line is called the Process Variation Zone and is delimited by prediction limits. The Process Variation Zone is wider than the data points it encloses and accounts for small non-linearity, measurement noise and intra-device process variations.

In contrast, the SWs labeled G shown along the bottom of Figure 2 are not proportional to the SWs in the other rows. In this case, the defect has produced regional variation in the SW of Vdd_2 due to its proximity to this supply rail. A much smaller amount of variation occurs in Vdd_7 due to the attenuation effect of the RC network. The lack of correlation in this pairing is illustrated by the outlier data point G in Figure 3. From the plot, it is clear that the behavior of this device is not characteristic to the norm defined by the prediction limits of the Defect-Free simulation experiments.

Based on this example, the pass/fail criterion under each test sequence is straightforward. Across all pairings of test points, if a test device generates a data point that falls outside of the Process Variation Zone for any pairing, the test device is defective. Although the same result was obtained for other pairing of test points in this experiment, this may not be the case for **all** test point pairings. This is the expected result since the variation generated by the defect is regional. Therefore, in the worst case, it may be necessary to analyze all pairing of test points in order to determine if the test device passes under the test sequence. Ongoing research is designed to determine the minimal number of test point pairs that must be analyzed.

In general, the regression line itself is characterized by data points gathered from nominal defect free devices and those with parameters skewed at the limits of the particular process used. In this way, the regression fit and corresponding prediction limits accommodates good devices which operate at extreme, but valid, process specification corners.

3.2.1 The Decision Criterion

The distance labeled “residual” in Figure 3 is the metric on which the pass/fail criterion is based. A residual is defined as the shortest distance from the data point (G in the figure) to the regression line. A properly stimulated defective device is expected to produce at least one data point with a residual larger than the distance between the regression line and a chosen prediction limit. It also follows that larger values provide greater confidence that the device is defective.

The prediction limits in Figure 3 are exaggerated to show their hyperbolic nature. Figure 4 shows two representative scatter plots from 49 simulation experiments using the test sequence and model for Bridging Experiment 6. 43 of the simulations were used to derive the regression line

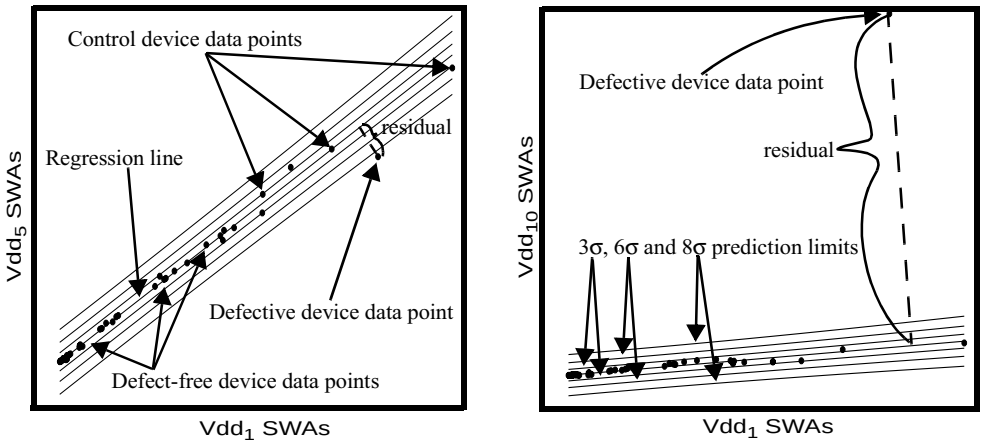

Figure 4. Scatter plots, regression lines and 3σ, 6σ and 8σ prediction limits using Fourier Magnitude data of Bridging Exp. 6 for Vdd1/Vdd5 (left) and Vdd1/Vdd10 (right).

and prediction limits. 5 control (defect-free) simulations and 1 defective simulation were also performed to evaluate these limits. The 3σ, 6σ and 8σ prediction limits are labeled in the plots and defined by

$$y = b_0 + b_1 x \pm W\sqrt{MSE}\sqrt{1 + \frac{1}{n} + \frac{(x-\bar{x})^2}{\sum_i (x_i - \bar{x})^2}} \quad \text{where} \quad W = \sqrt{2F(1-\alpha);2;(n-2)}$$

$$\sqrt{MSE} = \sqrt{\frac{\sum (Y_i - \hat{Y}_i)}{n-2}}$$

The prediction limits are sensitive to both the number of simulations or samples (1/n in the equation) and the amount of dispersion of the data points around the regression line (Mean Square Error or MSE). As explained in the next section, the number of simulations conducted for each experiment varied and is partially adjusted for through the use of different prediction limits. For this experiment, the 3σ limits bound the 43 data points used to derive the limits (as expected) but several of the control device data points fall outside of these limits. As explained in more detail in the result section, wider limits (6σ) are necessary to bound the dispersion of control data points for this experiment because the parameters to the model used to derive them were varied in such a way as to approximate worst case process drift.

In both of the scatter plots of Figure 4, the defective device data point falls outside the 8σ limits. However, the residual of the data point in the right plot more strongly indicates that this device is defective. Therefore, in addition to counting the number of data points that fall outside of the prediction limits in the set of scatter plots for an experiment, it is also meaningful to examine the magnitudes of the residuals. Instead of reporting on all of the residuals in each of the scatter plots individually, outlying data points such as the one shown in the right plot of Figure 4 are uncovered by computing the standard deviation of the residuals over all scatter plots for each device. In order to make this value meaningful for comparisons with other values, the magnitude of the residuals are normalized or standardized them using

$$\text{ZRES} = \frac{\text{residual}}{\sqrt{MSE}}$$

Here, MSE is the variance of the defect-free simulation residuals. The standard deviation is then

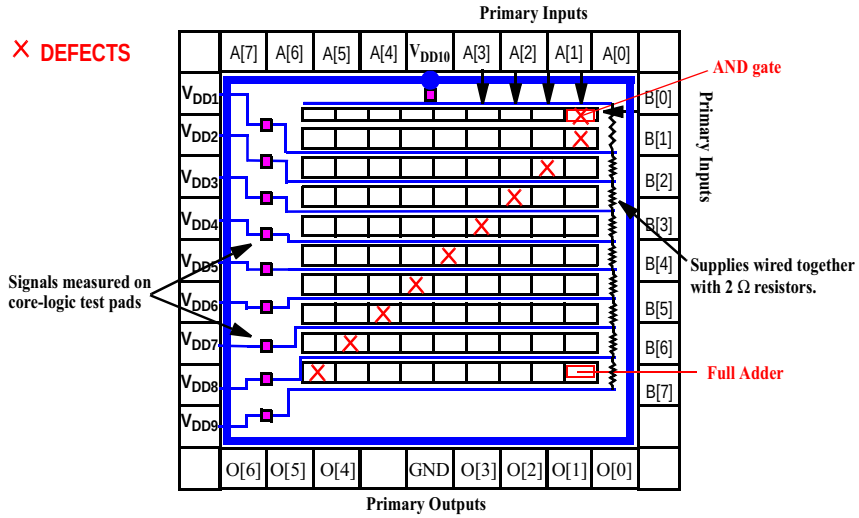

Figure 5. Block-level diagram of the multiplier showing defect locations.

computed as

$$\sigma_{res} = \sqrt{\frac{\sum_{i} (\mathrm{ZRES} - \overline{\mathrm{ZRES}})^2}{n-1}}$$

where the sum is computed over all scatter plots.

This value is computed for the control devices and the defective devices and compared. A large value for a defective device indicates that one or more of the residuals in the set of scatter plots is large such as the one shown in Figure 4 and the device can be easily identified as defective.

For the experiments in this paper, the prediction bands are used as the pass/fail threshold for the Test devices (both Control and Faulted) and the σ_{res} are used to evaluate the confidence of the prediction. In other words, a test device fails if at least one data point falls outside of a predetermined prediction band for any test point pairing. Moreover, the confidence that a test device is defective is higher for larger values of σ_{res}.

4.0 Experiment Setup

TSA experiments were conducted on a full-custom design of an 8-bit 2's complement multiplier. A block diagram of this device is shown in Figure 5. The primary inputs, labeled A[0] through A[7] and B[0] through B[7] are shown along the top and right of the figure. The power supplies for the core logic are labeled as V_{DD1} through V_{DD10} and are joined internally through a series connection of 2 Ω resistors (shown on the right in the figure) to simulate the supply grid configuration of a larger device. The transients were measured from the Metal2 core logic test pads (shown on the left in the figure), which is representative of conducting TSA at wafer probe. The input test sequences were run at 4 MHz for a duration of 250ns.

The regularity in the structure of the design made it possible to introduce defects at multiple locations while maintaining the ability to easily generate vector pairs which individually targeted a unique defect. The approximate locations of the defects are shown as 'X's in Figure 5.

Three versions of the multiplier were designed: a defect-free version, a version with 9 inserted shorts and a version with 9 inserted open defects. The resistance of the shorting defects in the bridging defective circuit varies between 0 Ω (hard short) and 10 KΩ. For the open defective multiplier, the range is 100 MΩ (hard open) and 2 KΩ.

4.1 Experiment Description

Accurate circuit models were generated using the SPACE extraction tool [18]. The lot averaged

	Reference Model	Defect-free Process Model. Training	Defect-free Process Model. Training	Defect-free Process Model. Training	Defect-free Control. Test	Defective Model. Test
Experiments	Br&Op1-9	Br&Op 1-3	Br&Op 4-6	Br&Op 7-9	Br&Op 1-9	Br&Op 1-9
# of models	1	37	43	22	5	2
Total # of sims	18	222	258	132	90	18
Transistor/Circuit parameters varied by +/− 5%, 10% and 25%	None	Beta, $V_{t,}$ poly Ω, metal2 contact Ω, metal cap. over p-/n-well	Beta, $V_{t,}$ p-/n-diff Ω, metal1 contact Ω, poly cap. to substrate, metal1 to metal2 cap.	All 9 parameters listed to the left.	All 9 parameters listed to the left.	None
# of circuit parameters varied per model.	None	1 (30 models). 9 (5 models). 9 at Min/Max (2 models).	1 (36 models). 9 (5 models). 9 at Min/Max (2 models).	9 (20 models). 9 at Min/Max (2 models).	9 (15 models).	None

Table 1: Simulation Experiments and Models.

circuit parameters reported by MOSIS for hardware devices fabricated at 2μ were used to derive the technology file used by SPACE. 18 bridging and open experiments were conducted, each dedicated to detecting exactly one of the 9 bridging or open defects.

A simulation run was made using a nominal defect-free simulation model and either a bridging or open defective simulation model for each of the 18 experiments. In addition, 81 simulation models were extracted from the layout and used to analyze the influence of process variations. In these models, one or more of the transistor and/or circuit parameters reported by MOSIS were varied over the range -25% and +25% of the nominal value.

Table 1 summarizes the simulation experiment models and runs. For example, in Bridging and Open Experiments 1-3 (column 3), models were extracted and simulated in which the parameters shown were changed individually for 30 models, and in groups of nine for 5 models by plus and minus 5%, 10% and 25% of the nominal values. Two additional simulations (Min and Max) were conducted for each of these experiments in which the nine process parameters were all set to -25% and +25% respectively to approximate the worst case process model.

The reference simulations identified in column 2 of Table 1 were used to create the Signature Waveforms as described in Section 3.1. The remaining simulations were divided into two groups, a Training group (columns 3 through 5) and a Test group (columns 6 and 7). The Training group was used to derive the regression lines and prediction intervals. The Test group was used to evaluate the prediction limits and the defect sensitivity of the method and are further divided into a Control group and a Faulted group.

The Control experiments (column 6) are defect-free simulations designed to approximate extreme cases of process drift and are used primarily to set the prediction limits for each of the three experiment groups. The limits were set such that no control data point fell outside of the prediction band. Since the number of simulations varied in the Training group across each of the experiment groups, 1-3, 4-6 and 7-9, it became necessary to set the σ value differently for each of these groups in order to keep the data points in the Control group bound within the prediction bands. The limits were set at 6σ, 8σ and 3σ for the three groups, respectively, to account for training set sizes of 37, 43 and 22 as shown in Table 1. Moreover, a different set of Control experiments were used for each of these experiment groups. The diversity in each of these groups also affected the appropriate σ value and emphasizes the necessity of choosing a training set that char-

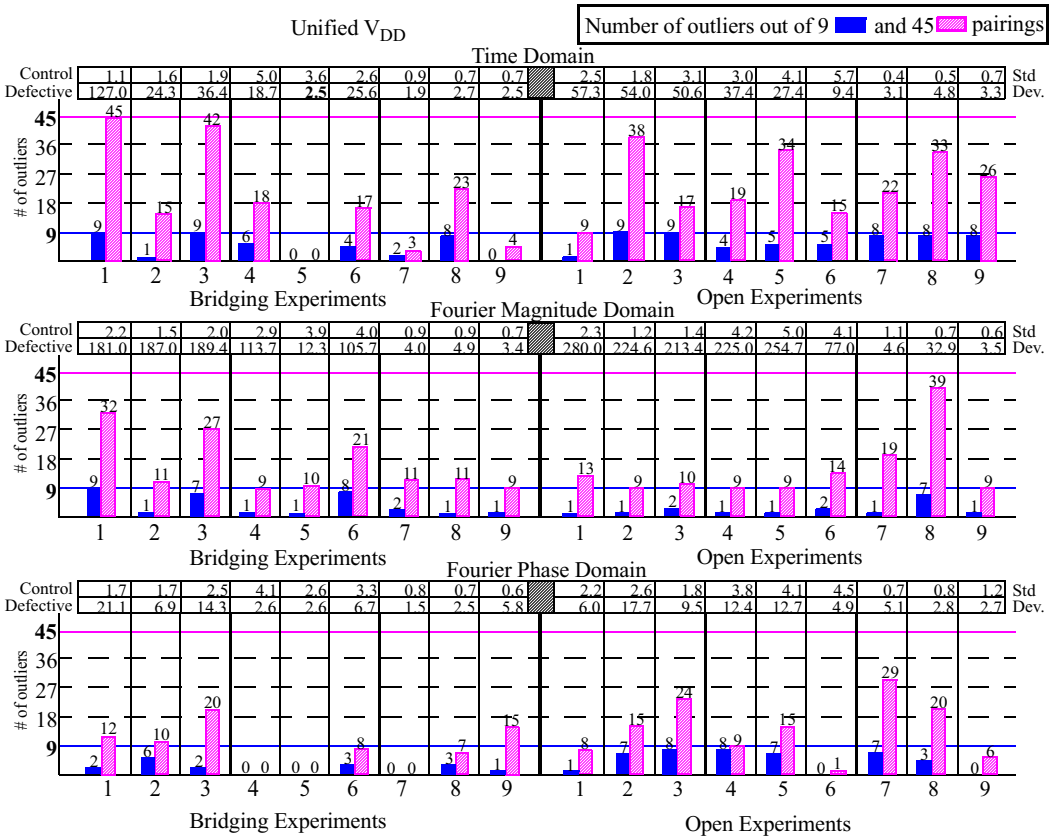

Figure 6. Time Domain, Fourier Magnitude and Fourier Phase Results.

acterizes the acceptable range of process drift.

The second set of simulations in the Test group (column 7) were run for each experiment using a model with a defect inserted and are the focus of the discussion given in the next section.

5.0 Experimental Results

The histograms of Figure 6 show the resulting number of "faulted" simulation data points which exceed the prediction limits for each of the 18 simulation experiments. The topmost histogram shows the results for the Time Domain analysis while the middle and bottom histograms show the results for the frequency domain (Fourier Magnitude and Fourier Phase). For each experiment, transient data was measured on each of the 10 supply rails simultaneously at the test points shown in Figure 5. Therefore, n*(n-1)/2 or 45 test point pairings are available for analysis under each experiment.

5.1 Outlier Analysis

The hatched bars in the histograms give the number of data points (out of a possible 45) that fell outside of the prediction limits while the solid bars give the number of outlying data points for a subset of these pairings: the 9 test point pairings involving Vdd_1 e.g. Vdd_1 and Vdd_2, Vdd_1 and Vdd_3, etc. As indicated in Section 3.2, a defect is detected if at least one data point falls outside of the prediction limits. In most cases, the subset of 9 pairings is sufficient to detect the defect. Since the complexity of the test is, in part, based on the number of pairings analyzed, these results indicate that only a subset of the pairings may be sufficient.

In all cases, the defect was detected in one or more domains. The analysis of the Fourier Magnitudes shows the best result in that all defects were detected using either 9 or 45 pairings. This is evident in the histogram as non-zero hatched and solid bars for all experiments. Moreover, no less than 9 outliers are generated in the larger group of 45 pairings. 6 of the experiments, e.g. Bridging

4 and 9, Open 2, 4, 5 and 9, give a value of 9 for the hatched bars. This occurs because the Vdd_{10} supply rail is very sensitive to the presence of the defects. The layout in Figure 5 shows that Vdd_{10} forms a ring around the core logic and may enable oscillations in defective circuits which are easily detectable.

The Time Domain histograms, although similar to the Fourier Magnitude, show larger numbers of outliers for most experiments. The similarity is expected since the total areas under the curves are theoretically identical. However, here there is a difference because the area of only the first 50 harmonics of the frequency domain were computed. The analysis of specific frequency range(s) may be useful in enhancing defect sensitivity and is currently under investigation.

The larger values in the Time Domain result primarily from higher correlations (99.9%) among the defect-free Training and Control simulations. This produces narrower prediction bands and makes it more likely that the defective device data points are outliers. In effect, these higher correlations increase the sensitivity of the test to defects.

The Time Domain results yield low values for Bridging Experiments 5, 7 and 9, however. The defect was undetected in nine pairings for experiment 9 and undetected in any pairing in experiment 5. The correspondence of these results with those obtained in the Magnitude indicate that these defects are, in general, more difficult to detect. This is partially explained by the higher resistance (8.7K and 10K Ohms, respectively) of the shorts for experiments 7 and 9. However, this is not the case for experiment 5 in which the resistance of the short is nearly 0. Other reasons for this anomaly are currently under investigation.

The Fourier Phase results are the least useful in this analysis. This contradicts the results obtained from previous hardware experiments and the simulation model is suspected as the main contributor to this inconsistency. However, positive detections occurred in all but three experiments and the best overall result was obtained in a few experiments, most notably Bridging experiment 9. This suggests that Phase may be more sensitive than Time and Magnitude to certain types of defects.

5.2 σ_{res} Analysis

The σ_{res} metric defined previously provides a means of evaluating the amount of variation produced by process shift and defects and, therefore relates to the degree of “observability” of the defect. σ_{res} is defined as the standard deviation of the residuals for each simulation across all test point pairings. Larger values indicate more dispersion in the data points and a higher degree of defect observability.

The maximum values computed from the Control simulations, as well as the value obtained from the Faulted simulations are shown along the top of each of the histograms in Figure 6. The range obtained for the Control experiments over all three domains is 0.4 to 5.7 while the range for the faulted simulations is 1.5 to 280. The range obtained for the Training simulations (not shown) is 1.1 to 3.1, which is comparable to the Control experiment results. This is the expected result if, in fact, the Training simulations “represent” the variation in the Control simulations. For example, the σ_{res} values for Bridging and Open experiments 7 through 9 are smaller than the values obtained in the other experiments across all three domains. However, the number of outliers is large in many cases. This indicates that the prediction bands are narrow and the Training simulations are effective in representing the variation in the Control simulations.

Several generalities can be made concerning the σ_{res} and outliers values. First, if a large σ_{res} is obtained, then one or more data points have very large residuals and the defect is easily detected. This occurs frequently in the Magnitude results, particularly in the first 5 Bridging and Open experiments. Secondly, if a small σ_{res} value is obtained, and the number of outliers is large, then the outliers are not far from the prediction bands. For example, the Time Domain results for Open

experiment 9 show a σ_{res} value of 3.3 and a value of 26 for the number of outliers. Lastly, if a small σ_{res} value is obtained, and the number of outliers is small, then the defect is difficult to detect. The Time Domain results for Bridging experiment 7 show an example.

5.3 Discussion

The simulation experiments performed indicate that the Magnitude analysis can identify defective devices without considering all 45 power supply cross correlations. Given a single reference supply (Vdd_1), 9 measurements were sufficient per circuit. Although the results are encouraging, it is difficult to definitively extrapolate the trend to large, more realistic sized circuits. One possibility is that more than one test point pairings will need to be considered because it is difficult to predict the effect of distance between the defect and the test points.

Notable in these simulation experiments is the high frequency of outliers across the experiments. This suggests that the analysis of fewer pairings may be sufficient to detect the defects in other designs. While it is difficult to claim that a single pair will be sufficient for large circuits, it is probable that the trend will persist and only a small set of pairs with perhaps a single reference point, is required. Further experiments are planned to investigate this aspect of the technique.

Also of significance is that all 3 domains detect the failed circuits with similar capability. The significance of this observation is that degrees of freedom are introduced into the methodology. That is, in a final implementation, one or all of the domains may be measured depending on their "defect sensitivity" and the practicality of the manufacturing solution. For instance, while each of these domains may, in fact, capture a specific characteristic of the circuit behavior, the relative performance of each domains to specific types of defects is unknown at this time. While it may be conjectured that each domain can target non-overlapping defect-types, the experimentation here is insufficient to judge this.

6.0 Conclusions

Transient Signal Analysis (TSA) is proposed as a means of identifying defects while compensating for process drift. The voltage transients at the power supply pins are measured and processed in the time and frequency (Fourier Magnitude and Phase) domains. These waveforms are transformed into a SWA, which is the area of the difference waveform constructed using the sampled transients of a test and reference device. The set of regression lines from scatter plots of SWAs from different Vdd pins comprise a profile of the parametric operation of a device.

Using regression analysis, defect free data (perturbed by simulated process variation) is used to determine a correlation profile characteristic of a "good" device. For experimentation, a failed circuit deviates from this profile by more than a fixed σ computed in advance from a set of defect-free devices that characterize acceptable levels of process drift. This method and criterion compensates for transient variations resulting from assumed process drift. This is a notable strength of the approach.

Simulation experiments were performed on an 8-bit multiplier to evaluate the effectiveness of the TSA procedure and its applicability to larger circuits. While it is difficult to prove that the current approach is directly transferable to realistic chips, the results do suggest that such investigation is not impractical. That is, it was shown that the injected defects were detectable using a small subset of the n^2 test point pairings.

The 3 domains explored provided similar defect detection capability but their relative effectiveness of targeting different defect types is yet unknown. However, the possibility of 3 alternatives to accomplish similar TSA tasks does offer flexibility in developing a practical production-oriented solution.

In the near future, improvements to the method will involve: minimizing the number of Vdd pairs cross correlated, investigation of self-relative measurements (which would eliminate the need for defect free references), experiments on real circuit products and formulation of a practical

implementation/approximation of the TSA technique.

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