

# ***Probing High Power Logic Die at Sort***

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## Agenda

- High Power – A Test Point of View
- How a Probe Card Affects Power Delivery
  - Space Transformer
  - PCB
  - Probes/Needles
  - Interconnects
- Improvements to the Probe Card
- Measuring the Probe Card
- Summary



## What is High Power?

- For this discussion, products that consume >> 30 Watts of power
  - 1998: Only a few server products (~10%)
  - 2001: All but a few products (~80%)
- Trends:
  - Voltages decreasing
  - Current demand is rapidly increasing
  - Power<sup>1</sup> is exponentially trending over time.

Year	Frequency	Current	Power	Voltage
1990	16 MHz	1 A	5 w	5 v
1993	66 MHz	3 A	10 w	3.3 v
1996	200 MHz	12 A	30 w	2.5 v
1999	600 MHz	50 A	90 w	1.8 v
2002	1200 MHz	150 A	180 w	1.2 v

Source: *Power Distribution System Design Methodology & Capacitor Selection for Modern CMOS Technology*. L. Smith, R. Anderson, D. Forehand, T. Pelc, T. Roy

<sup>1</sup> Power = Voltage\*Current



# Power Delivery

- **Goal #1: Stable Voltage during test**
  - Many devices require <10% voltage margin
  - Violation can cause false fails at testing
- **Why this is a challenge:**
  - Current demand (  $\Delta I$  ) is rapidly growing
  - Voltage margins decreasing

$$V = I * Z$$



$$Z = \frac{V}{I}$$

$$Z = \frac{\downarrow \Delta V}{\uparrow \Delta I}$$

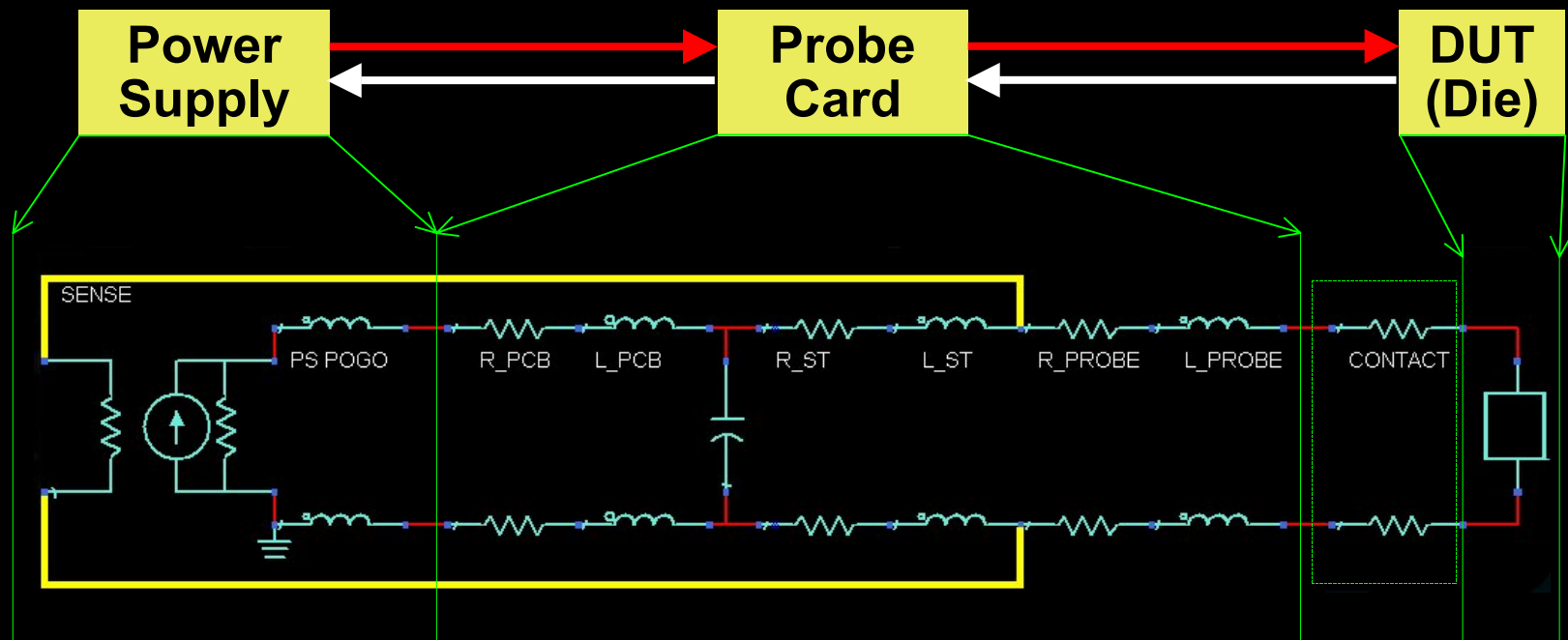
**Delta V drops**  
**Delta I rapidly grows**

**Impedance targets, Z, are reduced**



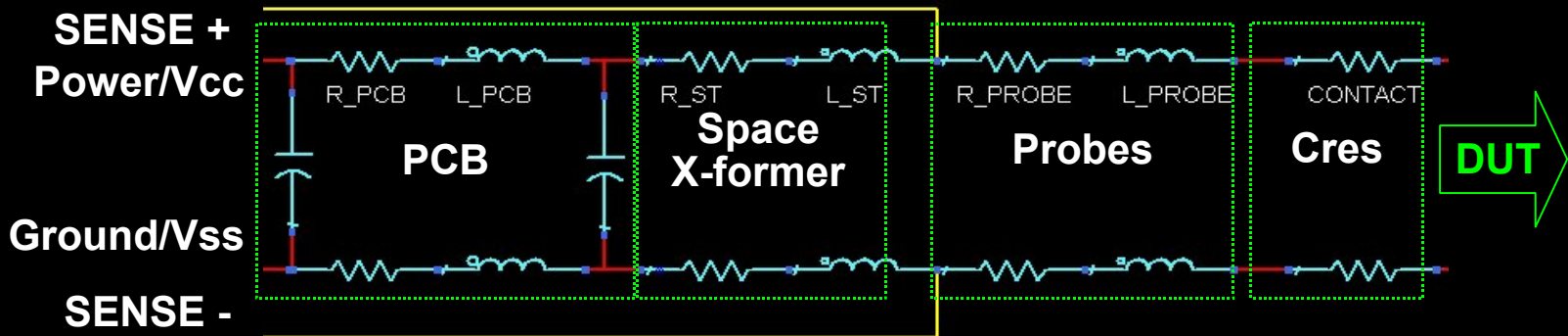
## Probe Card Impedance

- Impedance is analogous to resistance, but is a function of frequency  $Z \propto R(f)$ 
  - Loss of energy due to resistance
  - Storage of energy due to inductance and capacitance



# Probe Card Impedance

- Electrical view of the probe card
  - PCB & Space Transformer
    - » Metal planes
  - Probes & Contact Resistance
    - » Many (in parallel) wires
  - Capacitance



- Assumes C4 design
- Ignores interface between ST/PCB
- Ignores interface between PCB/PS



# Impedance Impacts

- PCB and Space Transformers

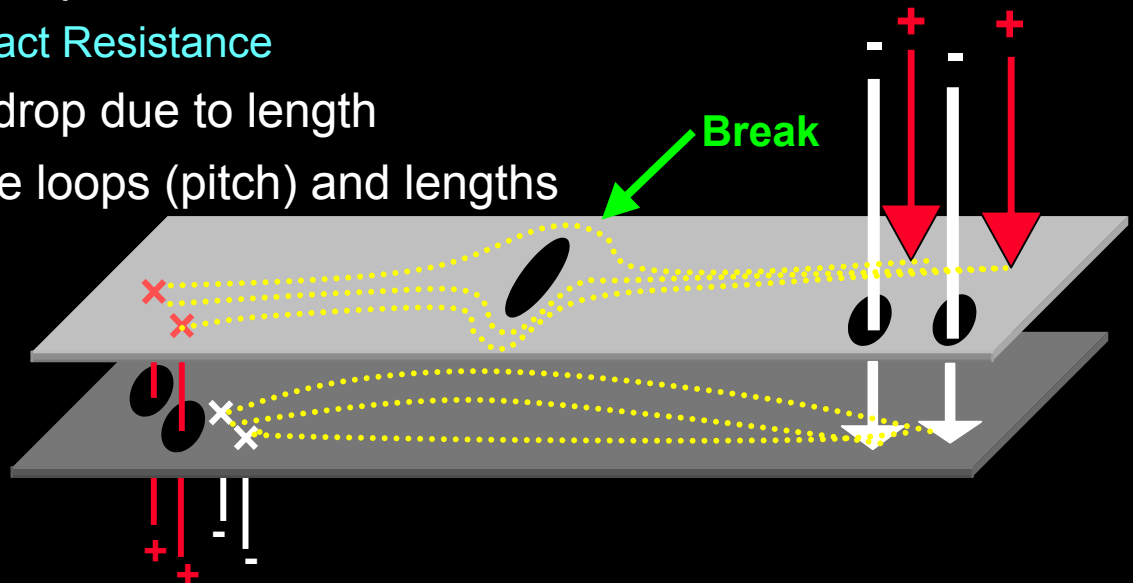
- Power plane distribution losses

- » R = Conductivity concerns (Ohms/square)
    - » L = Current flow impediments
      - Breaks in the planes (vias and mounting hardware)

- Interfaces

- BGA, Pogo Pins, Solder Joints, Interposers, Probes, etc.

- » R = DC drop at interfaces
      - Contact Resistance
    - » R = DC drop due to length
    - » L = Large loops (pitch) and lengths



## Improvements – Resistance

- **Reducing Overall Resistance**
  - Reduce Contact Resistance
    - » More Power and ground probes in parallel
  - Better Electrical Probes
    - » Shorter
    - » Better conductivity
  - Interfaces (BGA, probes to Space transformer, etc.) with better contact resistance
  - More Space Transformer Planes in Parallel
- **Some Resistance can be nullified by sensing**
  - Over time (milliseconds) the power supply can 'overdrive' the system voltage to null out resistance
  - Limitations exist as to how far into the system one can tap



## Improvements – Inductance

- **Reducing Inductance**

- Reduce interconnect inductance

- »  $L_{\text{SELF}}$  is a direct function of length
    - » Changes in interconnect wire diameter have a small impact
    - » Tighter pitches lend to reducing inductance
    - » Intercalating Power and Ground connections

- Reduce or remove breaks in the power planes

- » Places where power and ground paths are separated

- **Ground path is as important as Power path!**

- Equal and opposite currents travel in ground return



# Improvements – Capacitance

- **Selecting Capacitance**

- Location, Location, Location

- » Locate electrically close to DUT

- Quantity

- » Too little will diminish effect

- » Too much will load the circuit

- Quality

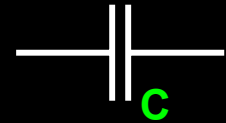
- » Capacitance has parasitic attributes as well

- ESR → Resistance

- ESL → Inductance

- » Use a Frequency domain analysis to better understand each

- **Pick capacitance understanding tradeoffs of ESR,ESL & C**



# Improvement Summary

- **Major areas of focus:**
  - Reduce (AND STABILIZE) Contact Resistance
    - » Shaped tips
  - Shrink interface geometries
    - » Reduce probe/needle lengths
      - Shorter interface means less R & L
  - Capacitor placement
    - » Allow for capacitors to be electrically close to DUT
    - » Focus on many parallel components
      - Reduces ESR & ESL
- **Secondary areas of focus:**
  - Reducing PCB and ST thickness
  - Intercalate any interface with multiple contacts
  - Tighter pitch interfaces
    - » Reduces the inductance

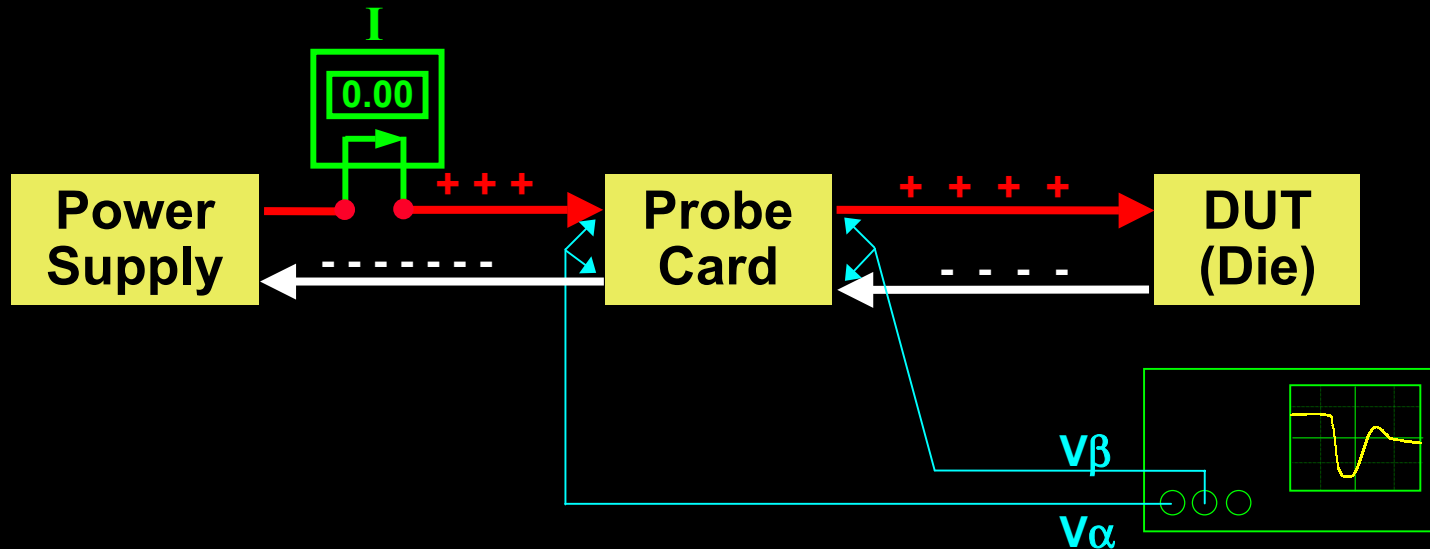


# Measuring Improvements

- **Two equivalent methods**
  - Impedance over the operating spectrum (Freq. Domain)
    - » Use a Low Impedance Analyzer
    - » Want to understand Impedance from DC to die demands
    - » Best for piecewise understanding
  - Measure Voltage under load (Time Domain)
    - » Measure the probe card under known load
    - » Best for system response understanding
- **Mix and match the two...**
  - Delve into the high impact items with piecewise models while still measuring full system response
    - » Superposition allows for piecewise measurements of the system



# One Method – Measuring a Probe Card



- Voltage drop =  $V_\alpha - V_\beta$
- Measuring current changes will determine DUT load/demand

**Remember:**

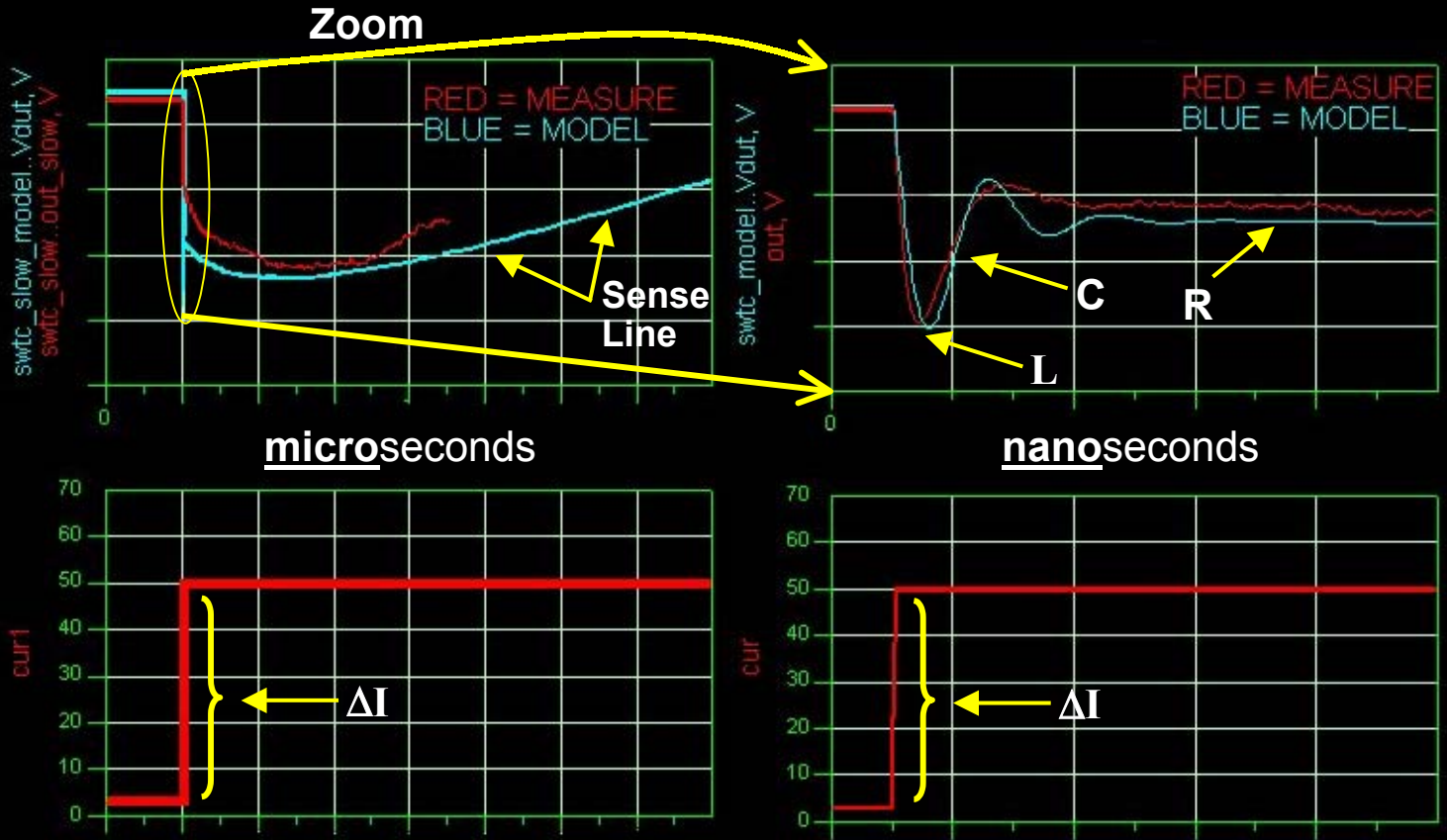
$$\text{Inductance} \rightarrow V_L = L * \frac{\Delta I}{\Delta t}$$

$$\text{Resistance} \rightarrow V_R = I_{DC} * R$$

$$\therefore \text{Voltage\_Drop} \rightarrow (V_\alpha - V_\beta) = (V_R + V_L)$$



# Measurements & Models



- This design has two distinctive droops
  - Due to placed capacitors
    - » One in nanoseconds (Right Top)
    - » One in microseconds (Left Top)



## Summary

- **Reduce impedance as power increases**
  - Reducing Resistance
  - Reducing Inductance
  - Strategically placing the right amount of capacitance
- **Areas of focus:**
  1. Reducing Contact Resistance
  2. Reducing Interface lengths
  3. Allowing for capacitor placement zones
- **Measure to validate changes**
  - Modeling is good, but limited to quality of input info
  - Superposition allows for piecewise measuring



**THANK YOU!**

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